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ELECTRICAL & COMPUTER ENGINEERING
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A Low-jitter Phase-locked Resonant Clock Generation and Distribution Scheme

by

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Abstract: Clock distribution networks have traditionally been optimized to minimize end-to-end delay of the distribution network.

However, since most digital ICs have an on-chip PLL, a more relevant design goal is to minimize cycle-to-cycle jitter. In this paper, we present a novel low-jitter phase-locked clock generation and distribution methodology which uses resonant standing wave oscillators (SWOs).

In contrast to traveling wave oscillator rings (TWOs or "rotary" clocks), our SWO achieves the same phase at every point in the ring, making it amenable to a synchronous design methodology. The standing wave oscillator is controlled by coarse as well as fine tuning. Coarse tuning is achieved by varying the ring inductance, while fine tuning is accomplished by varying the ring capacitance. Clock distribution is done by routing the resonant ring chip-wide in a "comb" like manner.

Experimental results demonstrate that the cycle-to-cycle jitter and skew of our approach is dramatically lower than existing schemes, while the power consumption is significantly lower as well. These benefits occur due to the resonant nature of our SWO-based clock generation and distribution approach.

Sunil P. Khatri received the B.Tech. degree in Electrical Engineering from the Indian Institute of Technology Kanpur, Kanpur, India, the M.S. degree in Electrical and Computer Engineering from the University of Texas, Austin, and the Ph.D. degree in Electrical Engineering and Computer Science from the University of California, Berkeley. He was with Motorola, Inc., for four years, where he was a member of the design teams of the MC88110 and PowerPC 603 RISC microprocessors. He is currently an Associate Professor with the Department of Electrical Computer Engineering, Texas A&M University, College Station. His research interests include logic synthesis, novel VLSI design approaches to address issues such as power, cross-talk, hardware acceleration of CAD algorithms, and cross-disciplinary applications of these topics. He has coauthored over 205 technical publications, 6 U.S. Patents, 9 research monographs, and 3 book chapters. Dr. Khatri was a recipient of four Best Paper Awards and five separate Best Paper Nominations.