Analog and Mixed-Signal Center
3128 TAMU
College Station, TX 77843-3128
Tel. (979) 845-9586
Fax. (979) 845-7161
E-mail:kentesar@ece.tamu.edu

ELECTRICAL & COMPUTER ENGINEERING
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S E M I N A R

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Use-it or Lose-it: Wearout and Lifetime in Future Chip-Multiprocessor Interconnect

by

Paul Gratz
Assistant Professor
Electrical and Computer Engineering
Texas A&M University

Abstract: Moore's Law scaling is continuing to yield even higher transistor density with each succeeding process generation, leading to today's multi-core Chip Multi-Processors (CMPs) with tens or even hundreds of interconnected cores or tiles. Unfortunately, deep sub-micron CMOS process technology is marred by increasing susceptibility to wear out. Prolonged operational stress gives rise to accelerated wear out and failure, due to several physical failure mechanisms, including Hot Carrier Injection (HCI) and Negative Bias Temperature Instability (NBTI). Each failure mechanism correlates with different usage-based stresses, all of which can eventually generate permanent faults. While the wear out of an individual core in many-core CMPs may not necessarily be catastrophic for the system, a single fault in the inter-processor Network-on-Chip (NoC) fabric could render the entire chip useless, as it could lead to protocol-level deadlocks, or even partition away vital components such as the memory controller or other critical I/O. In this talk, I develop critical path models for HCI- and NBTI-induced wear due to the actual stresses caused by real workloads, applied onto the interconnect microarchitecture. A key finding from this modeling being that, counter to prevailing wisdom, wear out in the CMP on-chip interconnect is correlated with lack of load observed in the NoC routers, rather than high load. A novel wear out-decelerating scheme is then developed in which routers under low load have their wear out-sensitive components exercised, without significantly impacting cycle time, pipeline depth, area or power consumption of the overall router. We subsequently show that the proposed design yields a 14-65X increase in expected CMP lifetime.

Paul V. Gratz is an Assistant Professor in the department of Electrical and Computer Engineering at Texas A&M University. His research interests include energy efficient and reliable design in the context of high performance computer architecture, processor memory systems and on-chip interconnection networks. He received his B.S.and M.S. degrees in Electrical Engineering from The University of Florida in 1994 and 1997 respectively. From 1997 to 2002 he was a design engineer with Intel Corporation. He received his Ph.D. degree in Electrical and Computer Engineering from the University of Texas at Austin in 2008. His paper "B-Fetch:Branch Prediction Directed Prefetching for In-Order Processors" was selected as one of four "Best Papers from IEEE Computer Architecture Letters in 2011". At ASPLOS '09, Dr. Gratz co-authored "An Evaluation of the TRIPS Computer System," receiving a best paper award. In Spring 2010, he received the "Teaching Excellence Award - Top 5%" award from the Texas A&M University System for a graduate-level Advanced Computer Architecture course he developed.