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S E M I N A R

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A 6-bit 10-GS/s TI-SAR ADC with Low-Overhead Embedded FFE/DFE Equalization for Wireline Receiver Applications

by

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Abstract: High-speed ADC front-ends in wireline receivers allow for implementing flexible, complex, and robust equalization in the digital domain, as well as easily supporting bandwidth-efficient modulation schemes, such as PAM4 and duobinary. However, the power consumption of these ADC front-ends and subsequent digital signal processing is a major issue. This paper presents a 64-way 6-bit 10-GS/s time-interleaved successive-approximation-based ADC front-end that efficiently incorporates a two-tap embedded FFE and a one-tap embedded DFE, providing the potential for a lower complexity back-end DSP and/or decreased ADC resolution. Fabricated in a 1.1V GP 65nm CMOS process, the ADC with embedded equalization achieves 0.48 pJ/conv.-step FOM, while consuming 79.1mW and occupying 0.33mm^2 core ADC area. The effectiveness of the embedded FFE and DFE is demonstrated with significant timing margin improvement observed for 10Gb/s operation over several FR4 channels.

Ehsan Zhian Tabasy received the B.S. degree from Ferdowsi University of Mashhad, Mashhad, Iran, in 2006, and the M.S. degree from the University of Tehran, Tehran, Iran, in 2009, both in electrical engineering. He is currently working toward the Ph.D. degree at Texas A&M University, College Station, TX, USA.

His research interests include high-speed analog and mixed-signal integrated circuit design, with special emphasis on data converters. Mr. Zhian Tabasy was the co-recipient of the 2012 Intel/Analog Devices/Catalyst Foundation CICC Student Scholarship Award.