



## TEXAS A&M UNIVERSITY

Department of Electrical and Computer Engineering

College Station, Texas 77843-3128

TEL (979) 845-9583 FAX (979) 845-7161

ella@ece.tamu.edu

http://amsc.tamu.edu

## S E M I N A R

Room 119A, ZEC

January 29, 2013 3:55-5:10 P.M.

### Sub-Nyquist Rate Receivers via Compressive Sensing: Theory, State-of-the-Art and Challenges

by

Dr. Sebastian Hoyos  
Analog Mixed-Signal Center  
Texas A&M University

**Abstract:** This presentation discusses the revolutionary theory of Compressive Sensing (sampling sparse signal representations below Nyquist rate and still getting nearly perfect reconstruction) and how quick the community has investigated its potentials, applications and fundamental trade-offs between sampling rate, dynamic range, analog and digital complexity, and power consumption.

The talk is centered around a prototype implementation developed in the speaker's research group, it's based *on a mixed-signal parallel compressive sensing architecture that realizes wideband spectrum sensing for cognitive radios* at sub-Nyquist rates by exploiting the sparsity in current frequency usage. Overlapping windowed integrators are used for analog basis expansion, that provides flexible filter nulls for clock leakage spur rejection. A sub-Nyquist rate sampling receiver architecture that exploits signal sparsity by employing Compressive Sensing (CS) techniques. The receiver serves as an Analog-to-Information Conversion (AIC) system that works at sampling rates much lower than the Nyquist rate. A parallel path structure that employs current mode sampling techniques is used. The receiver performance is quantified analytically. Useful and fundamental design guidelines that are unique to CS are provided based on the analytical tools. Simulations with a 90nm CMOS process verify the theoretical derivations and the circuit implementations. Based on these results, it is shown that instantaneous receiver signal bandwidth of 1.5 GHz and 44 dB of signal to noise plus distortion ratio (SNDR) are achievable. The receiver power consumption is estimated to be 120.8 mW. A comparison with state of the art high-speed ADCs reveals that the proposed approach improves the figure of merit by a factor of 3 if the signal exhibits a 4% sparsity.

**Sebastian Hoyos** received the B.S. degree in electrical engineering from Pontificia Universidad Javeriana (PUJ), Bogota, Colombia, in 2000, and the M.S. and Ph.D. degrees in electrical engineering from the University of Delaware, Newark, in 2002 and 2004, respectively. He was with Lucent Technologies Inc., Bogota, Colombia, from 1999 to 2000 for the Andean region in South America. Simultaneously, he was a lecturer with PUJ, where he lectured on microelectronics and control theory. During his M.S. and Ph.D. studies, he was with PMC-Sierra Inc., the Delaware Research Partnership Program, and the Army Research Laboratory Collaborative Technology Alliance in Communications and Networks. He was a Postdoctoral Researcher (2004-2006) with the Berkeley Wireless Research Center, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley. He joined Texas A&M University, College Station, TX in 2006 where he is currently an Associate Professor with the Department of Electrical and Computer Engineering. His research interests include telecommunication systems, digital signal processing, and analog and mixed-signal processing and circuit design.

