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S E M I N A R

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Reference Frequency Generation and related spurs in a Cellular Transceiver in 65nm CMOS

by

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Abstract A stable reference frequency is very critical for wireless applications. Crystal oscillators are used to generate the PLL reference frequency for cellular handset transceivers and reference clocks for phone peripherals such as GPS, WLAN, and Bluetooth. Digitally-controlled crystal oscillators (DCXOs) are lately being preferred for this purpose over the more traditional Voltage-controlled crystal oscillators (VCXOs) due to their lower cost, smaller board area, potentially higher tuning range, better noise immunity, easier implementation of Automatic Frequency Control loop in digital domain and digital pre-distortion of the frequency control signal to achieve a linear tuning curve. This talk is centered on such a DCXO clock system implemented in a 65nm digital CMOS technology for a GSM/GPRS/EDGE transceiver. One of the main features of the system presented is the elimination of the 32.768 kHz crystal traditionally used to generate the Real-time-clock (RTC) of the cellular phone by deriving 32.768 kHz from the 38.4MHz oscillator. The architecture and circuit design issues are discussed in some detail together with a brief explanation of the RTC generation. The measured performance of the DCXO is provided and compared to the published state-of-the-art. The second part of the talk concentrates on the important issue of reference frequency (F_{ref}) spurs caused by this DCXO and observed at the transmitter output in the first silicon prototype of the Transceiver. The main emphasis is placed on the laboratory debug effort of these spurs. The circuit solution adopted in the next silicon to reduce the F_{ref} spurs to acceptable levels is also presented.

Fikret Dülger received the B.S. and M.S. degrees in electronics from Istanbul Technical University (ITU), Istanbul, Turkey, in 1993 and 1996, respectively, and the Ph.D. degree in electronics from Texas A&M University, College Station, in 2002.

He was a Research Assistant with the Electronics and Communication Engineering Department, ITU, from 1993 to 1996. In 1994, he was a Design Engineer with the ETA ASIC Design Center, Istanbul, Turkey. He was a Research and Teaching Assistant in the Department of Electrical Engineering, Texas A&M University, between Fall 1996 and Spring 2002. From January 2002 to February 2009, he worked as a Design Engineer in the RF IC Design Group, Texas Instruments Inc.. and between February 2009 and April 2011, he worked as a Senior RF IC Design Engineer in Microtune Inc., Plano, TX. Since April 2011, he has been working as an RF IC Design Engineer in the Integrated Basestation Transceiver Group at Texas Instruments Inc.. In addition to being coauthor of numerous scientific papers in international journals and conferences, he is coauthor of a book titled *Integrated RF Building Blocks for Wireless Communication Transceivers* (Saarbrucken, VDM Verlag Dr. Mueller, 2008) based on his doctoral dissertation. His research and professional interests are in the area of analog circuit design for RF integrated circuits.