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S E M I N A R

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Design of a High-Performance Phase Locked Loop with Integer and Fractional Spurs Reduction Techniques

by

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Abstract: With the arrival of the fifth generation (5G) communication, phase locked loops used as frequency synthesizers have attracted enough attentions both from academia and industrial applications. A high-performance frequency synthesizer directly affects the dynamic range of a wideband system in many ways. The frequency synthesizer's spur performances, including integer and fractional spurs, indicate system's robustness over fast varying wireless environment with rich out-of-band information.

Detailed system considerations for implementation of a phase locked loop will be introduced. Properties of different phase locked loops will be summarized in this seminar. Above that, structures of different spur reduction techniques will also be summarized. Based upon the discussions and considerations above, a high-performance hybrid phase locked loop, which used charge pump calibration and time-to-digital converter (TDC) based filtering simultaneously, achieved integer spur and out-of-band fractional spur levels less than -108dBc and -95dBc respectively from silicon measurement results, in a 2 to 4 GHz frequency range. Details of spur reduction techniques will be introduced and compared with state-of-the-art results.

Junning Jiang (S' 17) has been pursuing his Ph.D. degree in Electrical and Computer Engineering in Analog and Mixed Signal Center, Texas A&M University, College Station, TX, since 2015. He worked as an analog engineering intern with Analog Devices Inc., Greensboro, NC, the Summer of 2014, where phase locked loop (PLL) design and verification was included. He also got involved with RF power amplifier (PA) design and calibration with Vidatronic, College Station, TX, as a summer intern in 2019. His research interests include RF front-end, PLL, PA and calibration methodologies in analog systems.