



SEMINAR

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A 32 Gb/s Simultaneous Bidirectional Source-Synchronous Transceiver with Adaptive Echo Cancellation in 28nm CMOS

by

Yang-Hang Fan
Texas A&M University

Abstract: A simultaneous bidirectional (SBD) transceiver employs an efficient voltage-mode driver with a resistor-transconductance (R-gm) hybrid to enable transmission and reception of data on a single differential channel at the same time. An FIR filter-based adaptive echo cancellation system that cancels both near-end and far-end echoes allows for the support of a wide range of channels, while a continuous-time linear equalizer efficiently compensates for channel loss. The quarter-rate source-synchronous transceiver utilizes a 5/4X phase interpolator-based clock and data recovery system to set the optimum data sampling point. Fabricated in 28nm CMOS, the 32Gb/s SBD transceiver achieves 1.83mW/Gb/s and compensates for up to 10.2dB loss.

Yang-Hang Fan received the B.S. degree in engineering and system science and the M.S. degree in institute of electronics engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2007 and 2009, respectively. He is currently pursuing the Ph.D. degree in electrical engineering with Texas A&M University, College Station, TX, USA. From 2011 to 2015, he was with Faraday Technology, Hsinchu, Taiwan, where he worked on the design of mixed-signal integrated circuits for high-speed wireline communication. Since 2016, he has been a Research Assistant with the Analog and Mixed Signal Center, Texas A&M University. During 2018, he is an intern with Hewlett Packard Enterprise, Palo Alto, CA, USA. His current research interests include mixed-signal integrated circuits and high-speed electrical and optical link circuits.