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ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY

S E M I N A R

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Design of Highly Linear and Wideband Front-end for Cognitive Radio and 5G Applications

by

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Abstract: The cognitive radio systems have drawn enough attentions both from academia and industrial application in recent years, which targets at improving the utilization of precious spectrum resources. A high throughput and frequency-agile front-end will reduce the sweeping time of the targeted bands, such as from 3 to 6 GHz, and benefit the efficiency of the cognitive radio system. Together with the fifth generation (5G) communication standards, there has been a demanding requirement for a RF front-end with higher baseband bandwidth, e.g. over 100 MHz. Basically, a front-end for cognitive radio and 5G requires higher bandwidth and improved linearity to be tolerant to stronger in-band and out-of-band components.

Detailed system considerations for implementation of a wideband system will be introduced. Properties of different RF front-end structures will be summarized in this seminar. Above that, structures of different low noise amplifiers (LNA) will also be summarized. Based upon the discussions and considerations above, a wideband and highly linear front-end, which was demonstrated on silicon, achieved in-band IIP3 and P1dB over 15.1 dBm and 3.0 dBm respectively, in a 3 to 6 GHz frequency range. A baseband bandwidth of 200 MHz and NF less than 5.8 dB at 3 MHz IF was also verified. Beyond the RF front-end, requirements for other components, such as circuits for baseband information processing and frequency generation will also be mentioned.

Junning Jiang (S' 17) received B.S. degree in Electrical Engineering, Southeast University, Nanjing, Jiangsu, China and M.S. degree in Electrical and Computer Engineering from NC State University, Raleigh, NC. Since 2015, he has been pursuing his Ph.D. degree in Electrical and Computer Engineering in Analog and Mixed Signal Center, Texas A&M University, College Station, TX. He worked as an analog engineering intern with Analog Devices Inc., Greensboro, NC, in Summer 2014, where phase locked loop (PLL) design and verification was included. He also got involved with RF power amplifier (PA) design and calibration with Vidatronic, College Station, TX, as a summer intern in 2018. His research interests include RF front-end, PLL, PA and calibration methodologies in analog systems.