Analog and Mixed-Signal Center
3128 TAMU
College Station, TX 77843-3128
Tel. (979) 862-4253
Fax. (979) 845-7161
E-mail: hoyos@tamu.edu

ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY

S E M I N A R

Room 1003 ETB

September 17, 2018, 1:50 – 2:50 P.M.

Design of Power Efficient Pipeline/Time-interleaved Analog-to-digital Converters

by

Dadian Zhou
Texas A&M University

Abstract: In recent years, the demand of portable electronic devices grows rapidly, including mobile phones, laptops, smart devices, etc. All of these devices have batteries providing limited power. Therefore, power-efficient designs for integrated circuits on those devices become a popular topic, e.g. highly power efficient ADCs. To follow the trend in the field of ADC design, two projects will be discussed in the seminar.

One of our projects is about a pipeline ADC with current-mode multiplying digital-to-analog converters (MDACs). The current-mode MDAC architecture is proposed and is compared with a conventional flip-around switch-capacitor MDAC. The residual amplifier in current-mode architecture will save large amount of power theoretically. The work eventually achieves 61.3-dB/75-dB SNDR/SFDR at 200MS/s with a sinusoidal input. The total power consumption is 8.4mW. The area of ADC core is 0.23 mm^2 and is fabricated in TSMC 40nm technology. The other research is the design of a time-interleaved ADC with background calibration. A novel architecture is proposed and a 4-channel time-interleaved ADC has been implemented by using 5 commercial ADC boards, 1 clock generator and an FPGA board. An particle swarm optimization (PSO) algorithm is applied to minimize the three main issues (gain mismatches, offset mismatches and timing skews) limiting the performance of a time-interleaved ADC. Background calibration using the PSO algorithm will be presented during the seminar.

Dadian Zhou (S' 17) received his B.S. degree in Telecommunication Engineering from Xi'an Jiaotong-Liverpool University, Suzhou, Jiangsu, China and earned his M.S. degree in Communications and Signal Processing from Imperial College London, London, UK. Since 2014, he has been pursuing his Ph.D degree in Electrical Engineering in Analog and Mixed Signal Center, Texas A&M University, College Station, TX, USA. He worked as an Analog Engineering Intern with NXP Semiconductors, Austin, TX, in Summer 2017 and Summer 2018, where he was involved in general purpose IO design and verification. He was a recipient of Broadcom scholarship in 2014. His research interests include data converters, calibrations for analog and mixed-signal systems, power management (LDO design) and IO design.