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ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY

SEMINAR

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A 0.8-to-1.2 V 10-to-50 MS/s 13-bit Subranging Pipelined-SAR ADC Using a Temperature-Insensitive Time-Based Amplifier

by

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Abstract: This paper presents an energy-efficient 13-bit 10-to-50 MS/s subranging pipelined-SAR ADC with power supply scaling. In the presented ADC, a SAR-assisted subranging floating capacitive DAC (CDAC) switching algorithm reduces switching energy along with enhanced linearity and speed in the first-stage SAR ADC. A following temperature-insensitive time-based residue amplifier realizes open-loop residual amplification without background calibration, while maintaining the benefits of dynamic operation and noise filtering. Furthermore, asynchronous SAR control logic employs a pre-window technique to accelerate SAR logic operations. The prototype ADC was fabricated in a 130 nm CMOS process with an active area of 0.22 mm^2. With a 1.2 V power supply and a Nyquist frequency input, the ADC consumes 1.32 mW at 50 MS/s and achieves SNDR and SFDR of 69.1 dB and 80.7 dB, respectively. The operating speed is scalable from 10 MS/s to 50 MS/s with a scalable power supply range of 0.8-to-1.2 V. Walden FoMs of 4.0–11.3 fJ/conversion-step are achieved.

Kyoohyun Noh received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea in 2004, and the M.S. degree in electrical engineering from University of California, Berkeley, CA, USA in 2010. He is currently pursuing the Ph.D. degree in Texas A&M University, College Station, TX, USA. His research interests include ADC, wireless power transfer, battery charging, and energy harvesting interface. Mr. Noh was the recipient of the fellowship from the Korea Foundation for Advanced Studies. He also received the fellowship from NXP, Eindhoven, Netherlands. He was one of the outstanding student paper award finalists in IEEE MEMS 2017.