Analog and Mixed-Signal Center
3128 TAMU
College Station, TX 77843-3128
Tel. (979) 458-4114
Fax. (979) 845-7161
E-mail:spalermo@ece.tamu.edu

ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY

S E M I N A R

Room 164 BLOC

October 20, 2016 3:55-5:10 P.M.

Design Considerations of Integrated Frequency Synthesizers in CMOS SOCs

by

Dr. Sheng Ye
Maxlinear

Abstract: Modern large scale SOCs combine high performance radio IP along with large ASIC content. Meanwhile the requirement for high performance PLLs put more constraints on the design with limited power supply choices, close proximity to noisy ASIC blocks and large variation of junction temperatures. Multiple standards requires multiple PLLs to coexist on the same SOC. Balancing the often conflicting needs among different IP blocks requires the frequency synthesizer to be designed and optimized at architecture level. This talk covers design considerations in the frequency synthesis of the modern CMOS SOC design including tradeoff in frequency coverage, tuning range, spur and coupling between different PLLs.

Dr. Sheng Ye received the Ph.D. degree in electrical engineering from the University of California at San Diego. Since the fall of 2003, he has been with MaxLinear Inc., Carlsbad, CA. where he is currently a technical director. His research interests include signal processing and RF/mixed signal IC design for communication systems.