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S E M I N A R

Room 164 BLOC

September 29, 2016   3:55-5:10 P.M.

A Low Power Digitizer for Back-Illuminated 3D-Stacked CMOS Image Sensor Readout with Passing Window and Double Auto-Zeroing Techniques

by

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Abstract: This work presents a high-performance digitizer based on column-parallel single-slope ADC (SS-ADC) topology for readout of a back-illuminated 3D-stacked CMOS image sensor. To address the high power consumption issue in high speed digital counters, a passing window (PW) based hybrid counter topology is proposed. In this approach, the memory cells in the digital counters of SS-ADCs are disconnected from the global bus during non-relevant timing. To address the high column FPN under bright illumination conditions, a double auto-zeroing (AZ) scheme is proposed. In this technique, the AZ process is employed twice at reset and signal level, respectively. The double AZ scheme not only allows the comparator to serve as a crossing detector around the common-mode level, but it also enables low-voltage comparator design. The proposed techniques are experimentally verified in a prototype chip designed and fabricated in the TSMC 40 nm low-power CMOS process.

Qiyuan Liu (S'14) was born in Liaoyang, Liaoning, China. He received the B.S. degree in microelectronics from Tianjin University, Tianjin, China in 2011. Since Fall 2011, he has been pursuing the Ph.D. degree in Electrical Engineering at the Analog and Mixed Signal Center (AMSC), Texas A&M University, College Station, TX, USA. In Spring and Summer 2013, he was an Analog IC Design Intern with Broadcom Corporation, Irvine, CA, where he worked on Phase Locked Loop (PLL) design. During Summer 2014, he was with TSMC, Austin, TX working on sloping Analog-to-Digital Converter (ADC) design for image sensing applications. His research interests include data converters, image sensing interfaces and power amplifiers.