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TEXAS A&M UNIVERSITY

S E M I N A R

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Optimized layout for Noisy High Power chips

by

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Abstract: The advent of power management ICs has necessitated new layout techniques that designers have to take into consideration when developing ICs. These are particularly important for high power and high voltage applications.

This presentation seeks to identify and highlight a number of "got yous" that typically cannot be simulated, but are critical in achieving optimal performance.

Tuli Dake received his EE BS degree from Kwame Nkrumah University of Science and Technology (KNUST) in Ghana and his MS from Texas A&M University, College Station in 2000.

He has a number of conference and Journal publications including Journal of Solid-State Circuits. He also has a number of patents to his name.

He is currently a Design Manager with the Battery Management Group at Texas Instruments and is a Senior IEEE member.