

## SEMINAR

Room 1037 ETB

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### **A 75 MHz BW 68dB DR CT- $\Sigma\Delta$ Modulator with Single Amplifier Biquad Filter and A Broadband Low-power Common-gate Summing Technique**

by

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**Abstract:** Higher data rates for new wireless standards demand sigma delta modulators with higher bandwidth requirements that correspondingly increase its power consumption. A wide bandwidth, power efficient continuous-time  $\Sigma\Delta$  modulator is presented. The modulator introduces a 3<sup>rd</sup> order filter implemented with a lossless integrator and a multiple-feedback single-amplifier biquad with embedded loop stability compensation. An active summing block is implemented with a common-gate amplifier followed by a transimpedance amplifier that achieves optimum bandwidth vs power consumption tradeoff, making it suitable for over GHz operation. Fabricated in 40 nm CMOS, and clocked at 3.2 GHz, the modulator achieves a signal-to-noise and distortion ratio (SNDR) of 64.9 dB over 75 MHz BW while consuming 22.8 mW of power. The obtained Walden's Figure of Merit is 106 fJ/conv-step.

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**Carlos Briseno-Vidrios** received the B.S degree in electrical engineering from the Instituto Tecnológico de Ciudad Guzman (ITCG), Ciudad Guzman, Mexico, in 2009. He has been working toward the Ph.D. degree in electrical engineering at Texas A&M University since 2010. During summer 2012 and 2014, he was an analog design intern at Silicon Laboratories, and during summer 2013, he was an analog-rf design intern at Broadcom. His research interest include low power wide band ADCs, ADC digital calibration algorithms.