Analog and Mixed-Signal Center
3128 TAMU
College Station, TX 77843-3128
Tel. (979) 458-4114
Fax. (979) 845-7161
E-mail:spalermo@ece.tamu.edu

ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY

S E M I N A R

Room 1037 ETB

November 3, 2015 3:55-5:10 P.M.

ADC-and-DAC-based Transceivers for 100Gb Ethernet

by

Jun Cao
Broadcom

Abstract: New Ethernet standards, such as 802.3bj, respond to the need for higher data rates over backplanes and copper cables to reach 100Gbps throughput. ADC-DAC-based transceivers enable advanced signal modulations and integrated DSP to combat channel impairments. Interleaved structure propels ADCs to higher speed while the mismatch calibration is the key to achieve better ENOB. Choice of sub-ADCs has a direct impact on the system performance such as power, latency and BER. While flash ADCs dominate 10GE applications, SAR ADCs are more widely used for 100GE. High-speed DAC is essential for modulation formats such as PAMx and provides precise multi-tap FIR for the transmitter. DACs at speeds higher than 10GSps are discussed and their application in PAM4 signaling is demonstrated, including a DAC integrated in a 802.3bj-compatible-transceiver that enables 36Gbps transmission over legacy low bandwidth channels.

Jun Cao (S'96-M'99-SM'14) received the B.S. degree in physics from Peking University in 1994, MSEE from the University of Michigan in 1996 and the Ph.D. degree in electrical engineering from UC Irvine in 2003. In 1999, he joined NewPort Communications as one of the leading designers for the world's first commercial 10G CMOS transceiver. Since 2000, he has been with Broadcom's analog group, currently as a Director and a distinguished engineer. He has published more than 30 journal/conference papers, with more than 20 in ISSCC/JSSC, on the topic of high speed transceivers and data converters. He also has more than 50 U.S. patents.