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TEXAS A&M UNIVERSITY

S E M I N A R

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A 25GS/s 6b TI Binary Search ADC with Soft-Decision Selection in 65nm CMOS

by

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Abstract: Serial link systems require high-speed low-resolution ADCs to enable flexible and complex equalization in the digital domain, as well as easily support bandwidth-efficient modulation schemes. Binary search ADCs provide a good balance between flash and SAR ADCs in terms of speed and power efficiency. This talk presents a 25GS/s 8-way time-interleaved binary search ADC that employs a soft-decision selection algorithm to improve metastability tolerance and relax T/H settling requirements. The T/H design is further relaxed with reduced loading from a new shared-input three comparator structure. Fabricated in GP 65nm CMOS, the ADC achieves 4.62-bits ENOB at Nyquist and 143 fJ/conv.-step FOM, while consuming 88mW and occupying 0.24mm^2 core ADC area.

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