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ELECTRICAL & COMPUTER ENGINEERING
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S E M I N A R

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A Compact Verilog-A Model of Silicon Carrier-Injection Ring Modulators for Optical Interconnect Transceiver Circuit Design

by

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Abstract: Optical interconnect system efficiency is dependent on the ability to optimize the transceiver circuitry for low-power and high-bandwidth operation, motivating co-simulation environments with compact optical device simulation models. This paper presents a compact Verilog-A silicon carrier-injection ring modulator model which accurately captures both non-linear electrical and optical dynamics. The device's electrical behavior is described by a p-i-n diode SPICE model, while the optical response is captured with a dynamic ring resonator model which considers the ring's cumulative phase shift. Experimental verification of the model is performed both at 8Gb/s with symmetric drive signals to study the impact of pre-emphasis pulse duration, pulse depth, and dc bias, and at 9Gb/s with a 65nm CMOS driver capable of asymmetric pre-emphasis pulse duration. The potential for 15Gb/s operation is shown by utilizing the presented model for optimization of the asymmetric pre-emphasis signal waveform.

Binhao Wang received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2008, and the M.S. degree in optical engineering from Zhejiang University, Hangzhou, China, in 2011. He is currently pursuing the Ph.D. degree in electrical engineering at Texas A&M University, College Station, TX, USA. His research interests include high-speed optical links and RF photonics.