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## SEMINAR

## Room 1003 ETB

September 23, 2014 3:55-5:10 P.M.

## High-Voltage and Negative-Voltage Design Techniques and Examples

by

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**Abstract:** This presentation serves as an introduction to using standard CMOS, drain-extended (DEMOS), and lateral diffusion (LDMOS) transistors to operate under high- or negative-voltage conditions. Examples will include a common-gate amplifier architecture for current sensing, a high-voltage push-pull output stage, and a negative voltage LDO.

**Erick O. Torres** is an Analog Design engineer at Texas Instruments since he completed his Ph.D. degree from the Georgia Institute of Technology, where he focused on low-energy circuits and power converters. Since joining TI, Erick has worked in many areas of analog design while focusing on its integration into large-scale, mixed-signal ICs. Examples include high-voltage linear and switching power regulators, low-offset and high-speed amplifiers, low-voltage transceivers, output buffers, and others.

**Susan Curtis** is a Senior Analog Design engineer at Texas Instruments and has been at TI since she graduated from Iowa State University. Susan's area of expertise includes high speed amplifiers, low noise amplifiers and mixed signal designs for communication, computing and mobile equipment. Over the past few years, Susan has focused on the integration of high voltage switching converters, high performance signal chain and dense digital logic on the same IC, while maintaining low noise.