

SEMINAR

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Segmented Linear RF CMOS PA for Wideband Wireless Communications

by

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Abstract: The power amplifier (PA) is the major power consumer in the RF transceiver, and the design and implementation of high efficient CMOS PA has been a very active research and development area. The 3G and 4G communication standards use high data rate, bandwidth efficient modulations that result in a high peak to average power ratio (PAPR), and thus linear transmitters are required. Also, because of the high PAPR in such modulations as orthogonal frequency-division multiplexing (OFDM), the probability density function (PDF) of the transmitted power peaks in the power back-off (PBO) region. However, the power efficiency of linear PAs reaches maximum at the peak output power, and drops drastically in the PBO region. If conventional linear PAs are employed to satisfy the linearity requirements of the advance modulation schemes, they would operate in a low efficiency region most of the time.

This talk presents a 1.9 GHz linear power amplifier (PA) architecture that improves its power efficiency in the power back-off (PBO) region. The combination of power transistor segmentation and digital gain compensation effectively enhances its power efficiency. A fast switching scheme is proposed, such that PA segments are switched on and off according to signal power, i.e. the proposed scheme makes the PA power consumption correlate with the power of the input signal. Binary power gain variations due to segmentation are dynamically compensated in the digital domain. The proposed solution overcomes the trade-off between efficiency and linearity by employing the digital predistortion technique. The PA is implemented in 40 nm CMOS process, it delivers a saturated output power of 35 dBm with 44.9% power-added efficiency (PAE) and linear gain of 38 dB. The adjacent channel leakage ratio (ACLR) at ± 5 MHz at a maximum linear output power of 31 dBm for a baseband WCDMA signal is -35.8 dBc.

Haoyu Qian was born in Beijing, China. He received his B.S. degree in Physics from Peking University in 2006, and the M.S. degree in Physics from Texas A&M University in 2009. He is currently pursuing the Ph.D. degree in electrical engineering at Texas A&M University.

His research interests include voltage regulator integrated circuit design such as low drop-out (LDO) regulator and switching-mode voltage regulator, and RF integrated circuit design such as frequency synthesizer and power amplifier.