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ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY

S E M I N A R

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A Single Parity Check forward Error Correction Method For High Speed I/Q

by

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Abstract: Some proposed high speed wireline communication systems make use of an ADC front end to allow a feedforward equalizer (FFE) to compensate for the frequency dependent loss of the channel. High precision ADCs are expensive in terms of power. The FFE block performs multiplication and addition operations at high speed and further increases the power consumption. A simple forward error correction method is proposed by which the ADC resolution and the equalizer complexity can be reduced. A single parity check code implemented together with a threshold detector can provide single error correction capability. With this error correction capability, the number of taps required in the FFE block is shown to be reduced to 3 taps from 6 taps for a channel with 15dB insertion loss at 5GHz frequency with the data rate being 20Gb/s. The effective number of bits (ENOB) required from the ADC is also shown to reduce to about 3.5 bits from 6 bits. The high rate of the code and the very simple decoder architecture make this error correction mechanism well suited for the wireline application.

The talk will also briefly cover some statistical modeling techniques relevant to high speed links which have been leveraged to implement the error correction technique.

Shiva Kiran received his B.E degree in telecommunication engineering from Bangalore Institute of Technology, Bangalore, India and an M.Tech degree in microelectronics and VLSI design from Indian Institute of Technology, Kharagpur, India. He then worked as a digital design engineer at Intel for a year. He is currently working towards a Ph.D degree at Texas A&M University, College Station, USA. His research interests are in system and circuit design for high speed I/O and statistical modeling techniques for high speed link systems.