

Analog and Mixed-Signal Center
3128 TAMU
College Station, TX 77843-3128
Tel. (979) 845-9586
Fax. (979) 845-7161
E-mail:kentesar@ece.tamu.edu



**ELECTRICAL & COMPUTER
ENGINEERING**
TEXAS A & M UNIVERSITY

SEMINAR

Room 1003 ETB

October 7, 2014 3:55-5:10 P.M.

QoS Driven Power Management for Chip Multiprocessors

by

Jiang Hu
Texas A&M University

Abstract: With end of Dennard scaling, designers are torn between insatiable performance needs and the fundamental limits of chip power density. In current designs, performance must typically be traded-off to achieve energy savings or, conversely, performance gains come with significant energy overhead. This talk presents a novel approach with the potential to achieve synergistic energy-savings and performance gain in chip multiprocessors. Resources shared by processor cores, such as on-chip interconnect and shared memory, play an increasingly critical role in determining the overall chip multiprocessor performance. Our key observation is that per-core dynamic voltage/frequency scaling (DVFS) can be used as a client regulation mechanism for Quality-of-Service (QoS) of the shared resources. As a result, energy savings are feasible with almost no performance cost; in fact some performance gain may be seen due to the better allocation of shared resources. Based on this observation, we propose a new DVFS technique inspired by TCP Vegas, a congestion control protocol from the IP-networking domain. We also propose an uncore (interconnect + last level cache) DVFS technique that is applied in conjunction with the QoS-driven core DVFS. For single- application cases, our techniques achieve 53% energy savings with less than 1% performance degradation on average. Some applications actually show a small performance improvement while still saving significant energy, indicating the power of utilizing DVFS as a means of QoS. We demonstrate that these results also hold for multi-application workloads.

Jiang Hu received the B. S. degree in optical engineering from Zhejiang University, China, in 1990, the M. S. degree in physics in 1997, and the Ph. D. degree in electrical engineering from the University of Minnesota in 2001. He was with IBM Microelectronics from January 2001 to June 2002. Currently, he is a professor in the Department of Electrical and Computer Engineering at the Texas A&M University. His research interest is on Computer-Aided Design for VLSI circuits and systems, especially on large scale circuit optimization, clock network synthesis, robust design, on-chip communication and chip power management. He received a best paper award at the ACM/IEEE Design Automation Conference in 2001, an IBM Invention Achievement Award in 2003 and a best paper award at the IEEE/ACM International Conference on Computer-Aided Design in 2011. He has served as technical program committee member for DAC, ICCAD, ISPD, ISQED, ICCD, DATE, ASPD, ISLPED and ISCAS, technical program chair and general chair for the ACM International Symposium on Physical Design, and associated editor for IEEE Transactions on CAD and ACM Transactions on Design Automation of Electronic Systems.