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Design of Energy-Efficient A/D Converters with Partial Embedded Equalization for High-Speed Wireline Receiver Applications

by

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Abstract: As the data rates of wireline communication links increases, channel impairments such as skin effect, dielectric loss, fiber dispersion, reflections and cross-talk become more pronounced. This warrants more interest in analog-to-digital converter (ADC)-based serial link receivers, as they allow for more complex and flexible back-end digital signal processing (DSP) relative to binary or mixed-signal receivers. Utilizing this back-end DSP allows for complex digital equalization and more bandwidth-efficient modulation schemes, while also displaying reduced process/voltage/temperature (PVT) sensitivity. Furthermore, these architectures offer straightforward design translation and can directly leverage the area and power scaling offered by new CMOS technology nodes. However, the power consumption of the ADC front-end and subsequent digital signal processing is a major issue. Embedding partial equalization inside the front-end ADC can potentially result in lowering the complexity of back-end DSP and/or decreasing the ADC resolution requirement, which results in a more energy-efficient receiver.

This work presents efficient implementations for multi-GS/s time-interleaved ADCs with partial equalization. First prototype details a 6b 1.6GS/s ADC with a novel embedded redundant-cycle 1-tap DFE structure in 90nm CMOS. The other two prototypes explain more complex 6b 10GS/s ADCs with efficiently embedded feed-forward equalization (FFE) and decision feedback equalization (DFE) in 65nm CMOS. Leveraging a time-interleaved successive approximation ADC architecture, new structures for embedded DFE and FFE are proposed with low power/area overhead. Measurement results over FR4 channels verify the effectiveness of proposed embedded equalization schemes.

Ehsan Zhian Tabasy received the B.S. degree from Ferdowsi University of Mashhad, Mashhad, Iran, in 2006, and the M.S. degree from the University of Tehran, Tehran, Iran, in 2009, both in electrical engineering. He is currently working toward the Ph.D. degree at Texas A&M University, College Station, TX, USA.

His research interests include high-speed analog and mixed-signal integrated circuit design, with special emphasis on data converters. Mr. Zhian Tabasy was a co-recipient of the 2012 Intel/Analog Devices/Catalyst Foundation CICC Student Scholarship Award.