Analog and Mixed-Signal Center
3128 TAMU
College Station, TX 77843-3128
Tel. (979) 845-9586
Fax. (979) 845-7161
E-mail:kentesar@ece.tamu.edu

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Statistical Modeling of Metastability in ADC-Based Serial I/O Receivers

by

Shengchang Cai
Texas A&M University

Abstract: For operation at high data rates over high-loss channels, ADC-based serial link receivers (Fig. 1) are being proposed due to their ability to perform equalization in the digital domain and support bandwidth efficient modulation schemes, such as PAM4 and duobinary. However, ADC-based receivers generally consume higher power than binary receivers because of the multi-GS/s ADC implementations. Therefore, power-efficient ADC structures employing binary search algorithms, such as SAR ADCs, are being considered in favor of flash ADCs which use a brute-force search algorithm. Despite potential power efficiency advantages, the binary search algorithm is inherently prone to comparator metastability, which can cause large conversion errors at the ADC output and degrade BER performance in ADC-based receivers. While time-domain simulations can show the impact of metastability error on BER performance, the number of bits required to validate typical BER targets ($<10^{-12}$) becomes prohibitive and makes time domain simulation impractical. Thus, efficient simulation approaches are desirable to guide system designers in ADC architecture choice and allow circuit designers to see the receiver-level impact of comparator performance.

This talk presents an ADC-based statistical modeling methodology to analyze the BER impact of ADC metastability errors. Metastability models are developed for two popular high-speed ADC structures: flash and asynchronous SAR (aSAR) ADCs. Different methods are investigated to model metastability error propagation through a digital feed-forward equalizer (FFE), with a detailed discussion on the proposed partial-bit mapping approach that generates the error probability density function (PDF) at the FFE output. This error PDF is inserted into a statistical link model to evaluate BER degradation due to metastability error, with simulations comparing the proposed statistical model and transient results.

Shengchang Cai received the B.S. degree in microelectronics from Fudan University, Shanghai, China in 2012. He is currently working toward the Ph.D. degree at Texas A&M University, College Station, TX, USA. His research interests include high-speed data converter design and statistical modeling techniques for high-speed link systems.