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ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY

S E M I N A R

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Design Techniques for Energy Efficient Multi-Gb/s Serial I/O Transceivers

by

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Abstract: Total I/O bandwidth demand is growing in high-performance systems due to the emergence of many-core microprocessors and in mobile devices in order to support the next generation of multi-media features. High-speed serial I/O energy efficiency must improve in order to enable continued scaling of these parallel computing platforms in applications ranging from data centers to smart mobile devices. The first work, a low-power forwarded-clock I/O transceiver architecture is presented that employs a high degree of output/input multiplexing, supply-voltage scaling with data rate, and low-voltage circuit techniques to enable low-power operation. The second work presents a low power serial link transmitter design that utilizes an output stage which combines a voltage-mode driver, which offers low static-power dissipation, and current-mode equalization, which offers low complexity and dynamic-power dissipation. Finally, it presents that a scalable quarter-rate transmitter employs an analog-controlled impedance-modulated 2-tap voltage-mode equalizer and achieves fast power-state transitioning with a replica-biased regulator and ILO clock generation. Capacitive-driven 2mm global clock distribution and automatic phase calibration allows for aggressive supply scaling.

Young-Hoon Song received the B.S. and M.S. degrees in electrical engineering from University of Texas at Arlington, TX, in the U.S.A. in 2002 and 2004 respectively. He is currently working toward the Ph. D. degree at the Analog and Mixed Signal Center (AMSC) in Texas A&M University. In 2008 and 2012, he was an intern at Broadcom in Irvine and at IBM T.J. Watson Research Center in Yorktown Heights. His research interests include mixed-signal integrated circuit design primarily as applied to power efficient serial link transceiver for high speed digital communications.