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S E M I N A R

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Fundamentals and Recent Advances on Continuous-Time Sigma-Delta Modulators

by

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Abstract: Recent developments in mobile computing and wireless internet have led to exponential growth in demand for portable computers and smart phones equipped with WLAN operating at different standards. The digital computing required by these gadgets is facilitated by process scaling that follows Moore's law and is expected to continue down to 10nm physical gate lengths. Various wireless standards have been developed over the years due to the high demand for faster data rate in portable wireless communications, which has pushed baseband bandwidths up to a few tens of MHz. When high-resolution continuous-time lowpass ΣΔ ADC architectures are selected for emerging products because of their efficiency, a wide bandwidth is essential in multi-standard applications to accommodate receiver bandwidth requirements.
In this lecture, the fundamentals will be revised and limitations due to clock jitter and presence of strong blockers will be quantified; technology trends will be highlighted. A top-down design approach is followed, starting with system specifications down to design issues of main blocks. Properties of main architectures are fully described. Stability, linearity and power consumption issues in SD Modulators are addressed. Also, out-of-band blocker effects on modulator's SQNR and loop stability as well as loop saturation effects due to agile blockers, usually not properly discussed neither in books nor in scientific papers, are covered. Even though multi-bit architectures have been successfully utilized in multi-MHz bandwidth designs, significant research efforts are devoted to the find efficient solutions for the remaining issues: better linearity, wider bandwidth, robustness to clock jitter and co-existence with other standards. In particular, the feedback DAC nonlinearity significantly affects the ADC performance because it directly adds error to the filter input signal and it is not noise-shaped. The foundations on SD modulators will be covered first and then we will elaborate on linearity limitations as well as jitter and blocker tolerance issues. Two case studies experimentally verified are presented to illustrate design issues and to give insights into the possibilities that exist for solving these contemporary challenges with analog hardware and software-based processing techniques.

Jose Silva-Martinez got his PhD degree from the Katholieke Universiteit Leuven, Belgium in 1992. He currently holds the rank of Texas Instruments Professor in Analog Engineering at the Department of ECE, Texas A&M University. Dr. Silva-Martinez is an IEEE-Fellow and member of the 2013-2014 CASS Distinguish Lecture Program. His record of publications show over 100 journals and 160 conferences, 2 books and 12 book chapters and 1 patent. He is co-author of the papers that received the 2011 Best Student Paper Award, IEEE MWCAS, the 2003 Best Student Paper Award, IEEE RF-IC, and recipient of the 1990 Best Paper Award, European Solid-State Circuits Conference (ESSCIRC). He got the 2005 Outstanding Professor Award by the ECE Department, Texas A&M University, 2005; co-Advised in Testing techniques the student who was Winner of the 2005 Best Doctoral Thesis Award, presented by the IEEE Test Technology Technical Council (TTTC), IEEE Computer Society.