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ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY

S E M I N A R

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A 10 Gb/s 2-IIR-Tap DFE Receiver with 35 dB Loss Compensation in 65-nm CMOS

by

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Abstract: Increasing serial I/O data rates over high-loss channels necessitates efficient approaches to Intersymbol interference (ISI) cancellation at the receiver. Decision feedback equalizer (DFE) is preferred over linear equalizers for its high equalization capability that can be achieved without noise amplification. However, DFE power and area consumption increase due to critical path timing and the large number of taps required to cancel ISI of high loss channels. In this seminar, a serial I/O DFE receiver employing 2-IIR tap for efficient long-tail ISI cancellation will be discussed. Several backplane channels characteristics are studied to determine the number of IIR filters and their time constants for efficient area and power consumption. A modified multi-input two-stage slicer allows for DFE summation to be performed directly at the slicer and for optimization of the first-tap IIR filter/mux feedback path for cancellation of the critical first post-cursor. Fabricated in GP 65-nm CMOS, the receiver occupies 0.0304 mm^2 area and consumes 9.9 mW while operating at a BER<10^{-12} for 10 Gb/s data passed over a 40-inch FR4 channel with 35 dB loss at 5 GHz.

Osama Elhadidy: received the B.Sc. and M.Sc. degrees in electrical engineering from Ain Shams University, Cairo, Egypt, in 2004 and 2009, respectively, and is currently working toward the Ph.D. degree in electrical and computer engineering at Texas A&M University, College Station, TX, USA.

From 2005 to 2010, he was a Development Engineer with Mentor Graphics, Cairo, Egypt. In summer 2012, he was a Design Intern with Rambus, Chapel Hill, NC, USA. In summer 2013, he was an Intern with Texas Instruments, Dallas, TX, USA. His research interests include frequency synthesizers and high-speed mixed-signal IC design.