



## SEMINAR

Room 1003 ETB

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### Low Distortion Class D Amplifier Design in Advanced Nodes

by

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**Abstract:** The ability of Class-D amplifiers to generate relatively large output power levels at high efficiencies renders them attractive in mobile audio applications, where battery life and low thermal dissipation are crucial. At the same time, integrating audio and power management into system-on-chip (SOC) is also attractive in order to reduce footprint, cost and increase functionality. This typically entails migrating into finer process technology geometries. However, the goal of migrating to deep nano-meter nodes is typically hampered by reduced power supply (which reduces available signal dynamic range), degraded analog transistor characteristics, including short-channel-effects, increased flicker noise, random telegraph noise and passive component performance. In this Seminar, prevailing state-of-the art Class D amplifier design techniques are reviewed. A prototype low noise and low distortion design employing a mostly digital feedback loop to address some of the above node limitations is discussed. Measured Silicon performance achieves 100dBA SNR and 0.0056% THD+N in a 55nm CMOS technology.

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**Martin Kinyua** received the B.S. degree from the University of Nairobi in 1992, the M.S. degree from Texas Tech University in 1997 and the Ph.D. from SMU, Dallas, TX, in 2004, all in Electrical Engineering.

From 1997 to 2007, he was with Texas Instruments, Inc., Dallas, as a mixed signal designer working primarily on high speed and high resolution Data Converters. Since 2008, he has been with TSMC Technology Inc., in Austin, TX, as a R&D Technical Manager and Designer. His research interests include low noise Data conversion circuits and techniques, Delta-Sigma converters for Audio Applications, Class-D Amplifiers, low noise CMOS image sensor readout circuits and DC-DC switching power management circuits. He has published several papers and has 32 patents issued or pending.