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S E M I N A R

Room 118 Civil Engineering

Monday, October 4, 2004, 2:00 p.m. - 2:50 p.m.

First Part:

The FVF: A Useful Cell for Low-Voltage Analog Design

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Abstract: Low voltage techniques will become usual techniques for analog and mixed-signal designers. There are several reasons:

- First of all, down-scaling of technologies leads to gate-oxide thickness only several nanometers thick, so that voltage supply has to be reduced down to 1.5 V, and below in the near future. However, threshold voltages do not scale in the same proportion. Many of the most common analog circuits do not work under these low voltage supplies, so that new design techniques are required to face this problem.
- Secondly, the extremely high density of integration characteristic of new technologies poses a severe problem in power dissipation. A natural way to reduce power consumption is to lower the supply voltage. Even though this power cut only applies for digital circuits, the reduction in the supply voltage also affects the analog part of the chip in a mixed-signal design.
- Finally, mobile and portable devices are based on batteries. In order to have an acceptable operation of a battery, low power and low voltage are mandatory.

In this talk, the Flipped Voltage Follower, a useful cell for low voltage analog design will be presented, along with a number of applications, ranging from very basic circuits (mirrors, amplifiers,…) to filters and VCO's.

Second Part:

Multirate Sigma-Delta Converters: An alternative to Multibits

Abstract: New high-speed sigma-delta (SD) analog to digital converters are required for xDSL and RF receivers. As sampling frequency is upper limited by the amplifier bandwidth and power consumption, these high-speed, low-power converters operate with a small oversampling ratio, using a unique sampling frequency. This paper shows that multirating is a useful technique to reduce power consumption in high speed SD modulators. To this end, three different multirate SD modulators are presented. The first and second ones use a low sampling frequency in the first integrator(s) of a single loop structure, while the third one uses a low oversampling frequency in the first stage(s) of a cascade converter.

Antonio Torralba is currently a Full Professor at the Electronics Engineering Department, University of Sevilla, where he is leading a research team in analog and mixed-signal design for communications and control. He is on leave for a 5-month stay in TAMU, starting January 2004. His research is focused in low-voltage / low-power analog design, and in A/D converters, especially Sigma-Delta converters. Prof. Torralba has published more than 40 papers in international journals and transactions and has participated in, and in some cases led, several international projects funded by the European Union through programs ESPRIT and IST, with different partners, such as AMS, ATMEL-ES2, ChipIdea, etc. Since 2001 he is also in charge of the Information Technologies Program of the Andalousian Research Council.