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## **S E M I N A R**

**Room 118 Civil Engineering**

Monday, November 15, 2004, 2:00 p.m. - 2:50 p.m.

### **ENCODING-BASED MINIMIZATION OF INDUCTIVE CROSS-TALK FOR OFF-CHIP DATA TRANSMISSION**

by

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**Abstract:** Inductive cross-talk within IC packaging is becoming a significant bottleneck in high-speed inter-chip communication. The parasitic inductance within IC packaging causes bounce on the power supply pins in addition to glitches and rise-time degradation on the signal pins. Until recently, the parasitic inductance problem was addressed by aggressive package design. In this work we present a technique to encode the off-chip data transmission to limit bounce on the supplies and reduce inductive signal coupling due to transitions on neighboring signal lines. Both these performance limiting factors are modeled in a common mathematical framework. Our experimental results show that the proposed encoding based techniques result in reduced supply bounce and signal degradation due to inductive cross-talk, closely matching the theoretical predictions. We demonstrate that the overall bandwidth of a bus actually increases by 85% using our technique, even after accounting for the encoding overhead. The asymptotic bus size overhead is between 30% and 50%, depending on how stringent the user-specified inductive cross-talk parameters are.

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**Sunil P Khatri** received his PhD. in EE from the University of California, Berkeley in 1999. He received his MS in ECE University of Texas, Austin in 1989 and his B Tech in EE from IIT Kanpur, India in 1987. He joined the EE department at Texas A&M University as an Assistant Professor in 2004. From January 2000 to June 2004 Khatri was an assistant professor with the Department of Electrical and Computer Engineering at the University of Colorado at Boulder. From 1989 to 1993, he worked with Motorola, Inc. on the designs of the MC88110 and PowerPC 603 RISC Microprocessors.

Sunil's research is in the areas of VLSI CAD (logic as well as physical design automation), VLSI Design (techniques to address specific Deep Submicron issues like cross-talk and power) and cross-disciplinary topics (Logic synthesis for quantum computing, VLSI implementation of LDPC codes, embedded systems design and scheduling approaches, VLSI applications in computer networking).

