

## TEXAS A&M UNIVERSITY

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## SEMINAR

Room 227A ZEC

Monday, January 24, 2005, 3:00 p.m. - 4:30 p.m.

## **Current Trends in Analog Design for SOC**

by

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**Abstract:** The design of analog circuit blocks for systems-on-a-chip is under constraints that are presently difficult, and in the future will be severe. Bandwidths and signal to noise ratios must be maintained in the face of decreasing power supply voltages, tighter supply current budgets, increasingly noisy substrate environments and shrinking devices with poor intrinsic analog processing capability. This presentation will summarize the current state of design techniques for maintaining acceptable analog performance within these constraints.

**John Fattaruso** grew up in Berkeley, CA, and received the B.S.(highest honors), M.S. and, Ph.D. degrees in electrical engineering from the University of California, Berkeley, through 1986.

He has been a Hertz Foundation Fellow, Teaching Associate, Research Assistant and Instructor at the University of California, Berkeley. In 1979 he worked in the Digital Signal Processing R&D group at Hewlett-Packard, Santa Clara, CA, and in 1985 he served as a consultant to Seeq Technology, San Jose, CA. Since 1987 he has been with various research and product development departments of Texas Instruments, Dallas, TX, working on analog VLSI technology. He was elected Distinguished Member of Technical Staff in 2001. His research interests include analog and RF circuit design, circuit simulation and optimization, neural networks and numerical analysis. He currently holds 24 patents in circuit design, has authored or co-authored 20 conference and journal papers, and has served on the analog program subcommittee of the ISSCC and as guest editor of the JSSC.

Dr. Fattaruso is a member of Eta Kappa Nu, Tau Beta Pi and Phi Beta Kappa.

