

# Applications of Multipath Transform-Domain Charge-Sampling Wide-Band Receivers

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**Abstract**—Transform-domain (TD) receivers expand the received signal over a basis set, and then operate on the basis coefficients. An analog computation of the basis coefficients efficiently parallelizes the signal for digital processing, relaxing the sampling requirements and enabling parallel digital processing at a much lower rate. Frequency-domain (FD) sampling, as a special case of TD sampling, has been proposed to parallelize the sampling process in broad-band communication receivers. The flexibility and scalability of TD receivers allow for the design of receivers that can cope with a large range of narrow-band and broad-band communications standards. A theoretical TD receiver design example is provided which is capable of processing GSM, Bluetooth, IEEE802.11g, Wimax, and UWB in just one configurable front-end. An example of spectrum sensing in cognitive radio is also provided.

**Index Terms**—Cognitive radio (CR), frequency-domain (FD) receiver, multistandard receiver, software-defined radio, transform-domain (TD) receiver.

## I. INTRODUCTION

DIGITAL deep-submicrometer CMOS schemes for wide-band receivers are highly desirable for their flexibility, scalability and programmability properties. However, while these technologies aid digital circuit design, they are not suited for the design of conventional analog circuits. Hence, there is a need to shift the complexity to the digital domain. This requires either front-end topologies where the analog-digital converter (ADC) is close to the antenna or analog circuit schemes that are intensively digital. Pushing the ADC towards the antenna imposes very high tracking bandwidths and dynamic ranges which becomes prohibitively expensive in wide-band applications. On the other hand, digital intensive RF front-ends not only take advantage of deep-submicrometer CMOS but also relaxes the ADC requirements. At this end, successful examples of narrow-band digital RF front-ends have been reported in [1]–[3], where switched  $G_m$ - $C$  filters and passive switched capacitor circuits are used to implement charge sampling FIR and IIR filters with built-in anti-aliasing capabilities. However, receivers that can cope as well with wide-band and ultra-wide-band (UWB) signals remain a major challenge for the realization of software-defined radio and cognitive radios (CRs).

Manuscript received August 14, 2007; revised December 7, 2007. This work was supported by the Communications and Networks Consortium sponsored by the U. S. Army Research Laboratory under the Collaborative Technology Alliance Program, Cooperative Agreement DAAD19-01-2-0011. This paper was recommended by Guest Editor W. A. Serdijn.

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Digital Object Identifier 10.1109/TCSII.2008.919480

This work presents transform-domain (TD) receivers, based on charge sampling, as a candidate for the implementation of high-performance wide-band and UWB RF receivers. The TD receiver parallelizes the front-end by expanding the RF input signal onto a set of basis functions. The expansion over a base function is accomplished via mixing with a locally generated signal and then integration over a time window. Each expansion requires a parallel path, and parallel sampling at the end of the integration time provides a set of coefficients that become the representation of the signal. Several advantages of this receiver front-end have been reported in [4] which will be discussed in a more practical way in this paper. We propose charge sampling circuit topologies for the implementation of the TD receiver. Specifically, we show how a switched  $G_m$ - $C$  filter structure can be modified to perform mixing with the base function, signal windowing and integration in a very compact fashion. This topology enables the realization of a multistandard receiver that not only works for narrow-band standards like GSM and Bluetooth, but also for very wide-band schemes like UWB. Due to parallel digital signal processing, each path operates only on a fraction of the signal bandwidth, thus relaxing the tracking bandwidth requirements and minimizing the power consumption of each sampling path. Further, longer integration windows lower the clock speeds providing robustness to jitter, which otherwise can impose a major limitation on the ADCs to achieve high dynamic range.

The remainder of this paper is organized as follows. Section II gives the background of the TD receiver. In Section III, the frequency-domain (FD) receiver as a particular case of TD receivers is introduced. Two applications of TD receivers are presented in Section IV, one is the software-defined-radio multistandard receiver and the other is for CR spectrum sensing. Conclusions are provided in Section V.

## II. TD RECEIVER BACKGROUND

TD receivers process the signal in the TD rather than in the time-domain. To accomplish the digital TD processing, the signal is partitioned in windows of duration  $T_c$ . These windows have an overlapping time of  $T_{ov}$ , which defines an overlapping ratio  $OVR = T_{ov}/T_c$ . Then, a set of  $N$  coefficients are computed in each window via signal expansion over the basis functions  $\Phi_n(t)|_{n=0}^{N-1}$ . If  $M$  windows are needed for digital signal processing, a total of  $MN$  expansion coefficients  $R_{m,n}|_{m=0}^{M-1}|_{n=0}^{N-1}$  are computed as

$$R_{m,n} = \int_{mT_s}^{mT_s+T_c} r(t)\Phi_n^*(t) dt \quad (1)$$

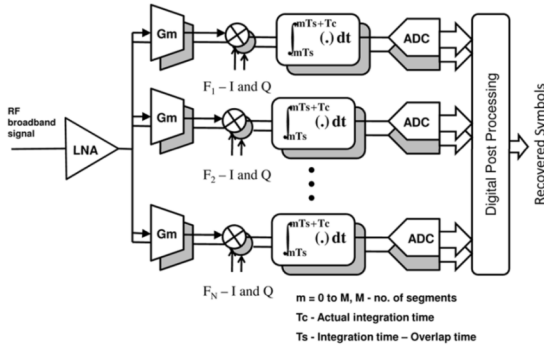


Fig. 1. Block diagram of FD receiver with  $N$  parallel paths.

where  $T_s = T_c - T_{OV}$ ,  $m = 0, 1, \dots, M - 1$ , and  $n = 0, 1, \dots, N - 1$ . At the end of each integration time  $T_c$ , the coefficients reach a value that is fed to an ADC for digitization. Finally, the quantized digital coefficients  $\bar{V}_{m,n} |_{m=0}^{M-1} |_{n=0}^{N-1}$  are sent to a digital signal processor (DSP) for further digital processing.

The basis functions determine the specific sampling transform domain. If sampling in the frequency domain is desired, the basis functions must be sinusoidal, or just square clocks in a hard switching implementation. The expansion coefficients become the Fourier series coefficients which will be referred in this paper as FD sampling. The signal information symbols can be reconstructed using FD estimators, including matched filter estimator, least square estimator and linear MMSE estimator [4]. Alternatively, when compressed sensing is applied, the basis functions can be random [5], [6], which will be briefly explained in Section IV as one potential application.

### III. FREQUENCY-SAMPLING RECEIVER

#### A. Structure of Frequency-Sampling Receiver

The FD basis coefficients are computed by mixing the input broad-band signal with LO signals followed by integration. Fig. 1 shows the block diagram of the FD broad-band receiver.

The  $G_m$  stages convert the input RF voltage signal into an RF current signal, which is downconverted to zero/low IF by passive mixers. This zero/low IF current is integrated onto a capacitor during the time window  $T_c$ . At the end of the integration window, the charge stored in the capacitor is the FD basis coefficient. As the capacitor is reset before the new integration window, the circuit does not behave as a continuous-time integrator. This is fundamentally different from traditional filter bank approaches where the filter has a continuous operation. An immediate advantage of the inherent resetting in the TD receivers is that sporadic interference does not propagate. The windowed integration of the input current signal also referred to as *charge sampling* has been analyzed in [7] and has been compared with the conventional voltage sampling. This windowed integration provides an inherent anti-aliasing *sinc* type filter that offers robustness to interference and aliasing of the out-of-band noise.

#### B. Multicarrier Receiver Example

In this section a system-level model is used to compare the performance of the charge sampling FD receiver and a conventional voltage-sampling based orthogonal frequency-division multiplex (OFDM) receiver in the presence of jitter. Jitter in

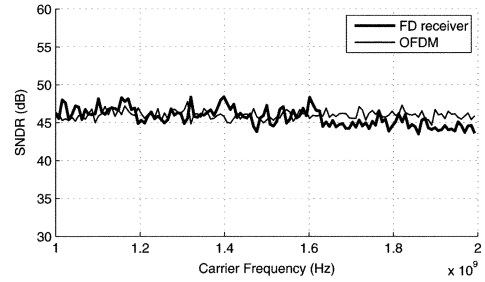


Fig. 2. Performance of FD receiver and OFDM in the presence of jitter with a second-order filter used after downconversion.

the mixing signals and clocks impose a fundamental limitation on the performance of the receiver. A theoretical analysis of the jitter in voltage sampling and charge sampling circuits is presented in [7].

The input to the system is a quadrature phase-shift key (QPSK) modulated signal of 128 carriers with bandwidth of 1 GHz from 1–2 GHz. The receiver model used in this example has 5 parallel  $I$  and  $Q$  paths. The quadrature mixing signals ( $I$  and  $Q$ ) used in each path form the basis functions. Their frequencies are chosen to be uniformly spaced around the center frequency of 1.5 GHz (1.1, 1.3, 1.5, 1.7, 1.9 GHz). The downconverted signals are filtered by a second-order  $RC$  filter with cutoff of 100 MHz. The fact that each path operates on a subband of the entire signal bandwidth is exploited in choosing the cutoff frequency of the  $RC$  filter. The output of the baseband filter is integrated over a time window of duration 5 ns. The integrated outputs form the FD basis coefficients that are processed digitally to recover the data. There is an overlap between successive integration windows for reasons explained in Section II which introduces oversampling in each path. The same multicarrier signal is applied to a conventional OFDM receiver. The OFDM system with a single  $I$  and  $Q$  path has a single square mixing signal at 1.5 GHz. The baseband filter is a second-order  $RC$  filter whose cutoff frequency is chosen to be 500 MHz to cover the entire signal bandwidth. The output of the baseband filter is sampled with the same amount of oversampling as the FD receiver. The detection of symbols is carried out using the FFT algorithm. Jitter with a standard deviation of 1 ps is introduced in both receivers. In the FD receiver, jitter is introduced in all the 5 mixing signals ( $I$  and  $Q$ ) and also at both edges of the integration window. In the OFDM receiver, jitter is introduced in the mixing signal and also in the sampling clock. Fig. 2 shows the comparison of the performance of FD receiver and OFDM. In this plot, signal-to-noise-distortion ratio (SNDR) of the recovered symbols is plotted across carrier frequencies. In this case, jitter in mixing signals and sampling clocks is the only source of distortion. It can be seen that the FD receiver shows no significant deterioration in performance despite the presence of more jitter sources. This is because of the superior anti-aliasing filtering in each path. The dominant jitter source in each path is the mixing signal at the center of the corresponding subband and the distortion from other jitter sources is mitigated by the filter. Due to parallelization, the sampling clocks are slower in the FD receiver than in the OFDM receiver. This translates to a greater jitter tolerance in the sampling clocks in the FD receiver. In the above example, for the same overall performance, the FD receiver can tolerate rms jitter of about 15 ps in the sampling clocks, but the OFDM

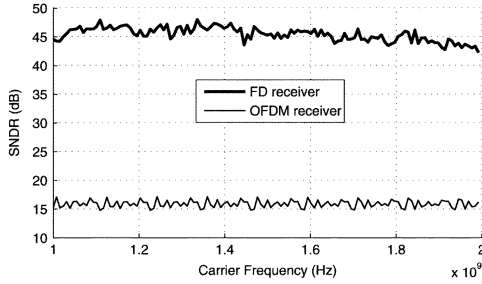


Fig. 3. Performance of FD receiver and OFDM in the presence of jitter without any baseband filter after downconversion.

receiver can tolerate only 5 ps of rms jitter. This results in considerable power savings in the design of buffers for the clocks in the FD receivers.

In order to demonstrate the additional anti-aliasing filtering provided by the windowed integration in FD receiver, the baseband anti-aliasing filters are removed in both the FD and OFDM receivers and the performance is analyzed in the presence of jitter. Fig. 3 shows the performance of the FD receiver and OFDM receiver in the absence of any baseband filter. It can be seen that while the FD receiver shows a marginal deterioration in performance, the performance of the OFDM receiver is significantly deteriorated. This shows that the baseband  $RC$  filter, mandatory in the OFDM receiver, can be eliminated for many applications when using the FD receiver, resulting in considerable savings in power and area.

### C. Receiver Front-End

A receiver front-end for the example discussed above is presented in this section.

The circuit of the low-noise amplifier (LNA) and driver for a single path is shown in Fig. 4. In the left side of the differential circuit,  $MP0$ ,  $MN0$ ,  $R0$ ,  $R2$ ,  $C0$ , and  $C2$  form the LNA.  $R0$  provides a wide band input impedance matching over the band of interest.  $MN2$  and  $MP2$  form the  $G_m$  stages.  $MN2$  and  $MN3$  are cross-coupled to cancel the noise coming from the LNA. The noise current of the LNA will flow through  $R0$ , generating correlated noise voltages at nodes A and B [8].  $MP2$  samples the noise voltage at B and  $MN3$  samples the noise voltage at A. They cancel each other if both paths have matched gains. On the other hand, the signal components are in opposite phase and add coherently. This topology helps to improve the noise figure (NF) which is usually high in deep-submicrometer CMOS technologies due to flicker noise. The NF is 6 dB before cancellation and 3–3.5 dB after cancellation.

As the LNA drives all the  $G_m$  stages, its bandwidth is limited by the total input capacitance of these stages. In simulations with 45 nm technology, the bandwidth of the LNA under this condition was found out to be 2.8 GHz which covers the band of interest. The LNA gain was 20 dB and the overall transconductance of  $G_m$  stages was 200 mS over the band. The power consumption is 9 mW for the LNA and 0.45 mW/mS for the  $G_m$  stages.

### D. Mixing, Windowing, and Integration

The computation of basis coefficients of the FD receiver needs the signal to be integrated onto a capacitor for a certain time window. As the incoming signal is passband, the flicker noise will not be a problem until the signal is downconverted to

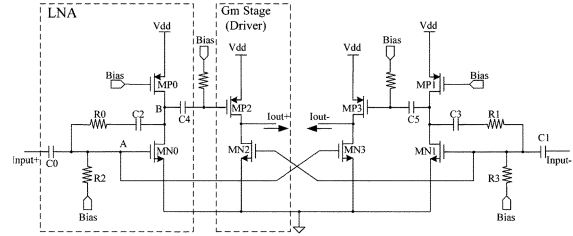


Fig. 4. LNA and driver stage in wireless front-end.

baseband. The  $G_m$  stage converts the signal into a current, then it is downconverted and integrated on the capacitors. Passive FET mixers are used for the purpose of downconversion as they offer low  $1/f$  noise and high linearity [2].

To minimize flicker noise of the mixer switches and improve linearity of the  $G_m$  stage, the swing at the output of the mixer must be minimized. Since the mixer is switching current, low voltage swing can be achieved by terminating the mixer output with a low impedance stage. There are at least two ways in which this can be done, using an active transimpedance amplifier or a common gate stage [2]. Both these circuits introduce flicker noise which can degrade the signal-to-noise ratio (SNR) performance of the zero/low intermediate frequency (IF) signal and have to be optimized.

A filter topology is introduced which exploits the overlap between successive charge samples and provides a better anti-aliasing filter. The sinc antialiasing filter is extensively used as an antialiasing and decimation filter in [1] and [2]. The  $\text{sinc}^2$  filter realized in [2] is used as a decimating filter after initial  $\text{sinc}$  filtering and it also uses a number of capacitors. Fig. 5(a) shows the single ended version of the filter which uses just one extra capacitor. An overlap of 33% is introduced between successive windows. All the capacitors have the same value and thus the effective integration window is the 0.5-1-0.5 window as shown in Fig. 5(b). This window can be seen as an approximation to a triangular window which has a  $\text{sinc}^2$  type of a filter response. Thus, the overlap effectively realizes a sinc antialiasing filter providing better attenuation and wider nulls. An ideal  $\text{sinc}$  and  $\text{sinc}^2$  filters are compared with the realized overlap  $\text{sinc}$  response in Fig. 6.

## IV. APPLICATIONS

### A. Software-Defined-Radio Multistandard Receiver

In this section, it is discussed how the FD receiver can accommodate multiple standards with varied bandwidths. Table I lists the specifications of some popular wireless standards.

The FD receiver provides a flexible tradeoff between speed, dynamic range and power consumption that makes it a candidate for a software-defined-radio multistandard receiver. Different speeds are achieved by varying the number of parallel paths used for signal expansion and quantization. Fig. 7 shows the block diagram of the multistandard receiver, the frequency allocation for the mixers and the reconfigurable anti-aliasing filter. The programmable anti-aliasing filter is exploited to achieve different filter specifications at different speeds. The reconfigurable ADC is a second-order sigma-delta modulator that is designed to operate in three different modes that trade power with maximum sampling speed. Reconfigurable sigma delta ADCs with sampling speeds upto 240 MS/s have been reported in [9]. The sigma delta ADC in this example is assumed to have a maximum

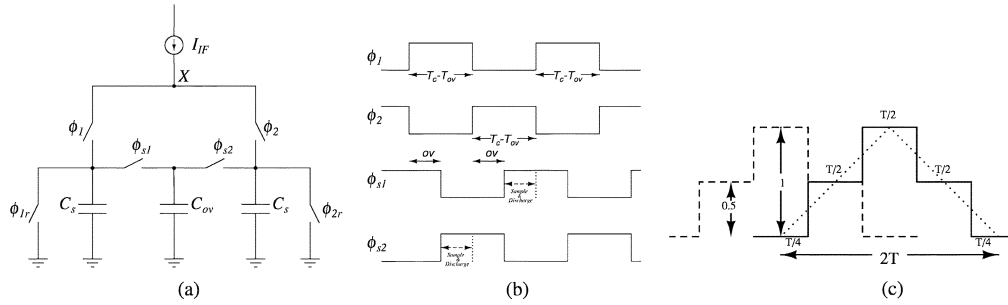


Fig. 5. Windowed integration with overlap. (a) Filter Schematic. (b) Clock Waveforms. (c) Triangular approximation.

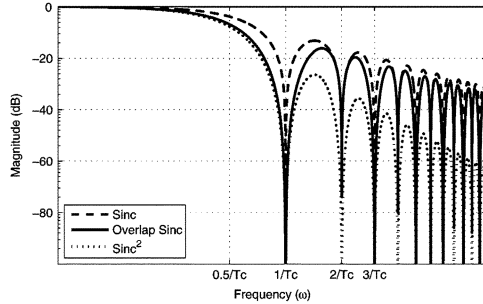


Fig. 6. Comparison of ideal sinc and  $\text{sinc}^2$  filters.

TABLE I  
SPECIFICATIONS OF THE POPULAR WIRELESS STANDARDS

Standard	Frequency Band	Bandwidth	Resolution
GSM	890-960kHz	200kHz	14 bits
Bluetooth	2.4GHz ISM	1MHz	12 bits
802.11b/g	2.4GHz ISM	20MHz	8 bits
WiMax	2 - 6GHz	25MHz	7 bits
UWB	3.1 - 10.6GHz	500MHz	5 bits

sampling speed of 500 MS/s achievable in deep-submicrometer technologies.

In the case of the UWB, all the five paths are activated to accommodate the huge bandwidth (500 MHz) of the UWB, a simple anti-aliasing  $\text{sinc}^2$  filter is used and the sigma-delta ADC is operated at its maximum sampling speed of 500 MS/s. Since the Nyquist speed of each path is 100 MS/s, the over-sampling ratio is sufficient to provide a resolution of 5 bits needed for the UWB. In case of 802.11b/g and WiMax, only one path is activated as the bandwidth of these standards (20 and 25 MHz) is much less compared to that of UWB. The anti-aliasing filter comprises of a  $\text{sinc}^2$  filter followed by a decimation filter that lowers the Nyquist sampling speed from 100 to 25 MS/s. The sampling speed of the sigma-delta ADC is reduced to 200 MS/s thus minimizing power consumption. In this mode, there is enough oversampling to provide a resolution of 8 bits for these standards. In the case of Bluetooth and GSM standards, a second decimation filter is used that lowers the sampling speed further. In these cases, the anti-aliasing filter must be designed such that the required level of image rejection and interference rejection is achieved even after decimation. This can be achieved by using an RC pre-filter or by employing an IIR filter [2], [10]. For Bluetooth, the sigma-delta ADC is operated at 200 MS/s, that achieves the 12-bit resolution. The ADC is operated at 20 MS/s for GSM as the bandwidth is only 200 kHz providing enough oversampling to achieve the required 14-bit resolution.

## B. CR Spectrum Sensing via Compressed Sensing

CR [11] provides a new paradigm to exploit the existing wireless spectrum efficiently. In CR, *spectrum holes* that are unoccupied by primary users can be assigned to appropriate secondary users. A reliable and efficient scheme to sense spectrum holes and detect primary users is a prerequisite to realize this dynamic spectrum access. However, due to the wide frequency bandwidth, potentially up to several gigahertz, spectrum sensing in CR can be a very challenging task. The advantages of TD receivers such as low sampling rate, robustness against jitter, flexibility and scalability make it fit for spectrum sensing in CR.

Moreover, much of today's spectrum usage is such that only a small portion of frequency bands are heavily loaded but others are partially or rarely occupied. Compressed Sensing (CS) [5], [6], a recent progress in mathematics, can be used as a framework to further reduce the spectrum sensing rate. According to CS theories, given a vector of discrete-time signal  $\mathbf{r}_{Q \times 1}$  that is  $K$ -sparse in some basis matrix  $\mathbf{\Xi}_{Q \times S}$ , i.e.,  $\mathbf{r} = \mathbf{\Xi}\mathbf{a}$ , where  $\mathbf{a}_{S \times 1}$  has only  $K$  non-zero elements, we can reconstruct the signal successfully with high probability from  $L$  measurements, where  $L$  depends on the reconstruction algorithm and is usually much less than  $Q$ . The measurement is done by projecting  $\mathbf{r}$  over another random basis  $\mathbf{\Phi}$  that is incoherent with  $\mathbf{\Xi}$ . The reconstruction is actually a  $l_1$ -norm optimization problem, which can be resolved by linear programming techniques or iterative greedy algorithms such as orthogonal matching pursuit (OMP).

Although CS was initially proposed for processing of discrete-time signal, it can be extended to processing an analog signal directly, where the random projection is done via mixers and integrators as in the TD receivers described in this paper. Note that the circuit topologies introduced here so far are directly applicable to these ideas. The only difference is that the clocks that drive the mixers need to be random or pseudorandom (PN). Bernoulli PN sequences can be used and can be implemented with digital sequential circuits.

In the following example, an OFDM-based CR system is considered. Suppose that there are  $S = 256$  subcarriers for primary users over the given wide frequency band and only  $K = 10$  randomly chosen subcarriers are used during each OFDM symbol period. TD receiver is used to detect the signal, where the basis functions are independent PN sequences and joint OMP is used to reconstruct the signal symbols. For simulations we use 1000 QPSK modulated OFDM symbols and a second-order Butterworth filter to reject the out of band noise. We assume perfect CSI and  $\text{SNR} = 10$  dB, and define the *perfect reconstruction rate* as one minus the *block error rate* of OFDM blocks and the *symbol error rate* as the error rate of QPSK symbols.

Fig. 8 shows how the number of parallel branches  $N$  changes with the number of samples per branch  $M$ , given the target

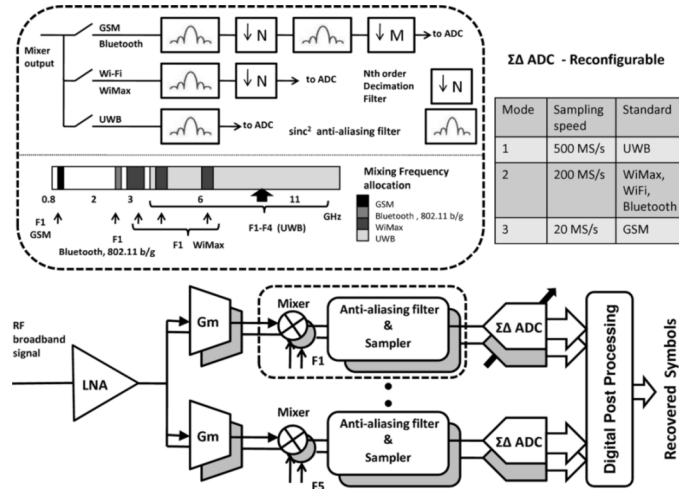


Fig. 7. Example of multistandard reconfigurable receiver.

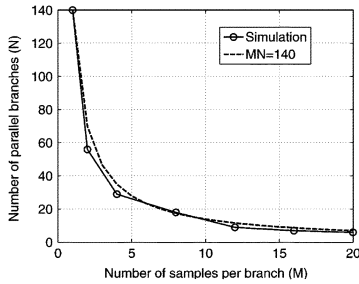


Fig. 8. Sensing rate vs system complexity in TD receiver based on CS given 95% perfect reconstruction probability.

perfect reconstruction rate of 95% which corresponds to a symbol error rate of  $10^{-4}$  approximately. Comparing the simulation curve with the dashed curve of  $MN = 140$ , we can make two important observations. First, the system works at subNyquist rate. If sampled at Nyquist rate,  $S = 256$  samples are needed for one OFDM symbol period  $T$ ; whereas in the proposed PSCS structure, each ADC needs to generate no more than 20 samples during each  $T$  and the total number of samples  $L = MN$  is approximately equal to 140 which is still less than 256. This significant reduction on the sensing rate is the benefit of parallelization and compressed sensing. Second, the number of parallel branches  $N$  is approximately inversely proportional to the number of samples per branch  $M$ , which presents a tradeoff between system complexity and sensing rate. For example, without segmentation, the sensing rate per branch is only  $1/256$  of the Nyquist rate, but over 100 parallel branches are required to have a satisfactory reconstruction. With 20 segments, only 8–10 parallel branches are enough, which is affordable for practical implementation, but the sensing rate is increased by 20 times.

## V. CONCLUSION

In this paper, we propose a structure of multipath TD charge sampling wide-band receivers that expand the received signal over a basis set, and then operate on the basis coefficients. The TD receiver with the advantage of subNyquist sampling rate and jitter robustness, provides a flexible and scalable topology for parallel digital signal processing, making it a candidate for software defined radio and CR. The FD receiver, as a special case of the TD receiver can be implemented with very simple

circuit topologies such as those proposed in this paper. When the signal has some sparsity over some basis, the TD receivers can be easily adapted to process the signal via compressed sensing by choosing random basis functions, an application example of which is the wide-band spectrum sensing in CR.

## ACKNOWLEDGMENT

Prepared through collaborative participation in the Communication and Networks Consortium sponsored by the U. S. Army Research Laboratory under the Collaborative Technology Program, Cooperative Agreement DAAD10-01-2-0011. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation thereon.

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