

A Noise Reduction and Linearity Improvement Technique for a Differential Cascode LNA

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Abstract—A typical common source cascode low-noise amplifier (CS-LNA) can be treated as a CS-CG two stage amplifier. In the published literature, an inductor is added at the drain of the main transistor to reduce the noise contribution of the cascode transistors. In this work, an inductor connected at the gate of the cascode transistor and capacitive cross-coupling are strategically combined to reduce the noise and the nonlinearity influences of the cascode transistors in a differential cascode CS-LNA. It uses a smaller noise reduction inductor compared with the conventional inductor based technique. It can reduce the noise, improve the linearity and also increase the voltage gain of the LNA. The proposed technique is theoretically formulated. Furthermore, as a proof of concept, a 2.2 GHz inductively degenerated CS-LNA was fabricated using TSMC 0.35 μm CMOS technology. The resulting LNA achieves 1.92 dB noise figure, 8.4 dB power gain, better than 13 dB S11, more than 30 dB isolation (S12), and -2.55 dBm IIP3, with the core fully differential LNA consuming 9 mA from a 1.8 V power supply.

Index Terms—Low-noise amplifier (LNA), capacitive cross-coupling, noise figure, noise reduction, linearity improvement, RF circuit.

I. INTRODUCTION

DUE to the low cost and easy integration, CMOS is widely used to design wireless systems especially in the radio frequency region. The low noise amplifier (LNA) serves as the first building block of the wireless receiver. It needs to amplify the incoming wireless signal without adding much noise and distortion. The noise performance of the LNA dramatically influences the overall system noise performance. The inductively degenerated CS-LNA [1]–[5] is widely used due to its superior noise performance. A common gate LNA (CG-LNA) can easily achieve the input impedance matching, but suffers from poor noise performance [6]. The capacitive cross-coupling technique for CG-LNA [7]–[9] partially cancels the noise contribution of the common gate transistor at the output, which improves the noise performance of the CG-LNA. On the other hand, due to the existence of the parasitic capacitance at the source of the cascode transistor, the cascode transistor's noise influences the overall noise performance of the CS-LNA [10]–[14]. In [13], a layout technique to merge the main transistor and the cascode

transistor can reduce the cascode transistor noise contribution. Additional inductors can be added at the drain of the main transistor to cancel the effect of the parasitic capacitance, thus improving the noise performance of the LNA [10]–[12] at the cost of larger area for the on-chip inductors.

In this paper, a noise reduction inductor combined with the capacitive cross-coupling technique is proposed to improve the noise and linearity performance of the differential cascode LNA. It can reduce the noise and nonlinearity contributions of the cascode transistors with a smaller inductor compared with the typical inductor based technique [10]–[12]. The capacitive cross-coupling technique used in the cascode transistors increases the effective transconductance of the cascode transistors, further improves the linearity of the LNA, and also reduces the Miller effect of the gate-drain capacitance of the main transistor.

Section II describes the basic inductively degenerated CS-LNA, analyzes the noise influence of the cascode transistors, and shows the conventional inductor based noise improvement technique. Section III discusses the original capacitive cross-coupling technique [7]–[9] for CG-LNA, and proposes its application combined with inductor in the cascode transistors of the differential cascode CS-LNA. It also gives the theoretical foundations of the LNA noise reduction with the proposed technique. Section IV discusses the LNA linearity improvement with the proposed technique. Section V addresses the effects of the proposed technique on the LNA S11 and gain. The measurement results are presented in Sections VI and VII provides conclusions. Detailed analysis of noise, linearity and voltage gain are presented in the Appendixes.

II. BACKGROUND AND PREVIOUS WORK

The LNA noise performance dominates the overall noise performance of the receiver. The inductively degenerated CS-LNA is widely used due to its superior noise performance.

A. Inductively Degenerated CS-LNA

The typical inductively degenerated CS-LNA is shown in Fig. 1, where all parasitic capacitances other than the gate-source capacitances of M_1 and M_2 are ignored for simplicity. It uses an inductor L_s to generate the real impedance to match the input impedance to 50Ω , which results in good noise performance [1]–[4]. If the resistive losses in the signal path, the gate resistance, and the parasitic capacitances except gate-source capacitances are ignored, the overall input impedance of CS-LNA can be simplified to (1), where g_{m1} is the transconductance of M_1 .

$$Z_{in}(s) \approx sL_g + sL_s + \frac{1}{sC_{gs1}} + g_{m1} \frac{L_s}{C_{gs1}} \quad (1)$$

Manuscript received April 3, 2007; revised November 29, 2007. Fabrication of the prototype IC was supported by MOSIS through its educational program.

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Digital Object Identifier 10.1109/JSSC.2007.916584

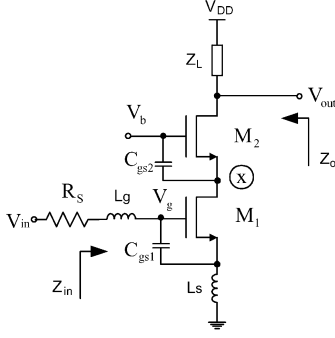


Fig. 1. Inductively degenerated cascode CS-LNA.

The small-signal model of the inductively degenerated cascode CS-LNA is shown in Fig. 2, where C_{gd} and g_{mb} of the transistors are ignored for simplicity. The capacitor C_x represents all the parasitic capacitances at node X. It is estimated as

$$C_x \approx C_{gs2} + C_{sb2} + C_{db1} \quad (2)$$

If the noise contribution from the cascode stage is ignored, the noise factor of the cascode CS-LNA becomes [1]–[4]

$$F_1 = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha} \frac{\chi}{Q_L} \frac{\omega_o}{\omega_T} \quad (3)$$

$$\chi = 1 - 2|c| \sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma} (1 + Q_L^2) \quad (4)$$

$$Q_L = \frac{\omega_o(L_s + L_g)}{R_s} = \frac{1}{\omega_o C_{gs1} R_s} \quad (5)$$

$$c = \frac{i_{g1}^{*2}}{\sqrt{i_{g1}^{*2}}} \approx -0.395j \quad (6)$$

where R_s is the input voltage source resistance, R_l represents the series resistance of the inductor L_g , R_g is the gate resistance of M_1 , ω_o is the operating frequency, and α , γ , and δ are bias-dependant parameters [1]–[4]. The existence of the parasitic capacitance C_x reduces the gain of the first stage, which makes the noise contribution from the cascode stage (F_c) larger. Thus, the noise factor of the cascode CS-LNA [11] becomes

$$F = F_1 + F_c \approx F_1 + 4R_s\gamma_2g_{do2} \left(\frac{\omega_o^2 C_x}{\omega_T g_{m2}} \right)^2 \quad (7)$$

where $\omega_T = g_{m1}/C_{gs1}$, g_{do2} is the zero-bias drain conductance of M_2 and γ_2 is the bias-dependent factor. Same as in [11], the noise sources of the first stage include the gate induced noise and drain noise sources, but only the drain noise of the second stage is modeled [7]–[11]. From (2) and (7), it can be observed that C_x increases the noise factor of the LNA.

B. Existing Solution to Reduce Noise

The parasitic capacitance C_x can be reduced by merging the main transistor and the cascode transistor in the layout [13]. In [10]–[12], an additional inductor L_{add} was added to cancel the effect of C_x at the frequency of interest. As a result, if the r_{o1} and r_{o2} of M_1 and M_2 are large enough, the noise current generated by the cascode transistor M_2 adds negligible noise current to the output.

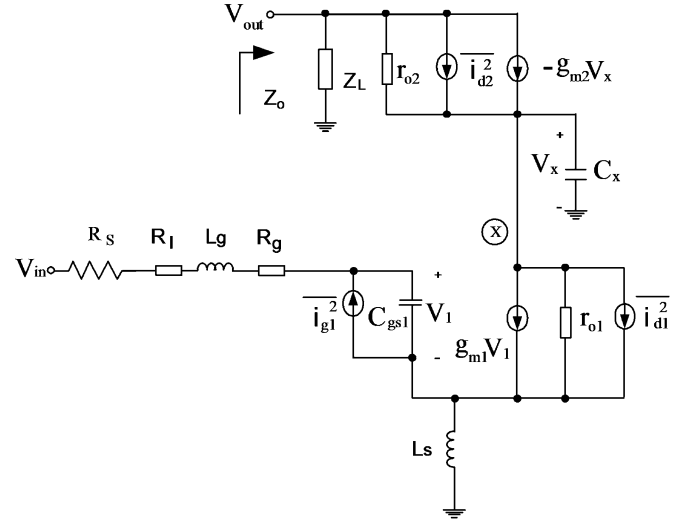


Fig. 2. Small-signal model of cascode CS-LNA for noise analysis.

The large area requirement of on-chip inductor is a big concern for on-chip integration. For a typical $0.35 \mu\text{m}$ CMOS technology, the parasitic capacitance for a $200 \mu\text{m}/0.4 \mu\text{m}$ nMOS transistor is nearly 0.3 pF . Thus, it requires an inductor around 14 nH to resonate at 2 GHz . In the advanced CMOS technology, it requires even larger inductor values. In addition, the poor quality factor of the on-chip inductor increases the overall noise figure of the LNA.

In this paper, we propose a technique to significantly reduce the noise and nonlinearity contribution of the cascode transistors as well as the value of L_{add} .

III. LNA NOISE REDUCTION WITH THE PROPOSED TECHNIQUE

The CG-LNA can achieve wideband input impedance matching, but suffers from poor noise performance. To alleviate this problem, a capacitive cross-coupling technique was proposed in [7]–[9] for CG-LNA. It can boost the transistor transconductance with passive capacitors, as shown in Fig. 3. If the gate-bulk and gate-drain capacitances are ignored, the effective transconductance and input capacitance of the LNA are here derived as:

$$G_{m,\text{eff}} = \frac{2C_c}{C_{gs} + C_c} g_{m1} \quad (8)$$

$$C_{\text{in}} = \frac{4C_c}{C_{gs} + C_c} C_{gs} = 2 \frac{G_{m,\text{eff}}}{g_{m1}} C_{gs}. \quad (9)$$

When $C_c \gg C_{gs}$, the effective transconductance is doubled, and the input capacitance is increased by four times.

The inductively degenerated cascode CS-LNA can be considered as a CS-CG two stage LNA. The CS stage is designed to achieve the input impedance matching and also to obtain best noise performance. The input voltage signal is converted to current through the CS transistor. The cascode transistor works as a CG stage. It is designed mainly to reduce the Miller effect of the parasitic gate-drain overlap capacitance in the CS transistor. It also helps to increase the output impedance and to improve the input–output isolation.

An additional inductor L_{add} combined with the capacitive cross-coupling technique is applied to the cascode transistors of

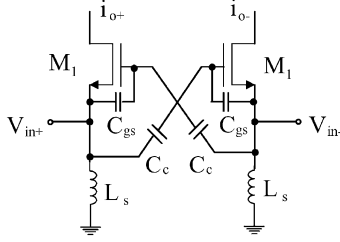


Fig. 3. Capacitor cross-coupled differential CG-LNA.

the differential LNA to reduce the noise. The proposed topology is implemented in a fully differential inductively degenerated CS-LNA as shown in Fig. 4. The input admittance at node X is given by $G'_{m,\text{eff}}(j\omega) + jB'_{\text{eff}}(j\omega)$, where the effective transconductance of the cascode transistor is expressed as

$$G'_{m,\text{eff}} = \frac{2\omega C_c - \frac{1}{\omega L_{\text{add}}}}{\omega C_c + \omega C_{gs2} - \frac{1}{\omega L_{\text{add}}}} g_{m2} \quad (10)$$

Note that in our proposed approach, the cross-coupled capacitors are applied to the cascode transistors. The equivalent input susceptance at node X is not purely capacitive, which can be derived as

$$B'_{\text{eff}} \cong \frac{4\omega C_c}{\omega C_c + \omega C_{gs2} - \frac{1}{\omega L_{\text{add}}}} \omega C_{gs2} + \frac{(\omega C_c + \omega C_{gs2}) \times \left(-\frac{1}{\omega L_{\text{add}}}\right)}{\omega C_c + \omega C_{gs2} - \frac{1}{\omega L_{\text{add}}}} + \omega C_{db1} + \omega C_{gd1} + \omega C_{sb2} \quad (11)$$

where other parasitic capacitances are ignored. From (10), if $\omega C_c \gg \omega C_{gs2}$ and $\omega C_c \gg \omega C_{gs2} - (1/\omega L_{\text{add}})$, the effective transconductance is doubled and the equivalent susceptance from (11) becomes

$$B'_{\text{eff}} \cong \frac{\omega C_c \left(4\omega C_{gs2} - \frac{1}{\omega L_{\text{add}}}\right)}{\omega C_c + \omega C_{gs2} - \frac{1}{\omega L_{\text{add}}}} + \omega C_{sb2} + \omega C_{gd1} + \omega C_{db1}. \quad (12)$$

At $\omega = \omega_o$, when (12) equals to zero, the capacitive effect at node X is mainly eliminated, which leads to

$$L_{\text{add}} \approx \frac{1}{\omega_o^2 (4C_{gs2} + C_{sb2} + C_{gd1} + C_{db1})}. \quad (13)$$

Using the small-signal model, the noise figure of the cascode LNA yields

$$F' = F_1 + F'_c = F_1 + 4R_s \gamma_2 g_{do2} \left(\frac{\omega_o B'_{\text{eff}}}{\omega_T G'_{m,\text{eff}}} \right)^2. \quad (14)$$

Note that B'_{eff} is a function of ω .

Since the effect of the parasitic capacitance at node X is cancelled as shown in (11)–(13), the noise of the cascode transistors, F'_c , is negligible.

The inductor L_{add} can be implemented with either on-chip inductor or bonding wire inductor. Its value is reduced by a factor of 4 with respect to the typical inductor based technique

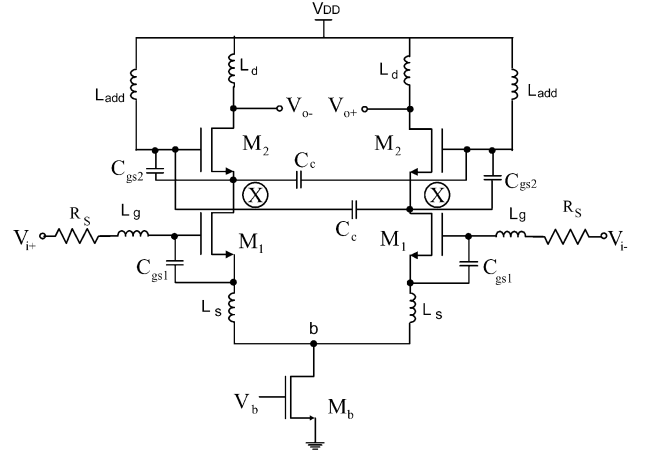


Fig. 4. The inductor combined with capacitive cross-coupling technique in a fully differential cascode CS-LNA.

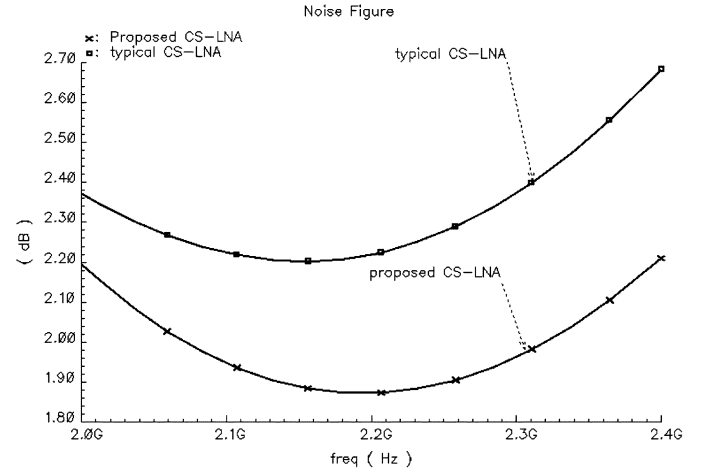


Fig. 5. Simulation results of the differential cascode CS-LNA with and without L_{add} and C_c .

[10]–[12]. Here L_{add} is implemented as a bonding wire inductor. Since now the gates of M_2 are connected out of the chip using the bonding wire inductor, it is desired to add ESD protection structures for these pads. In this design, to verify the proposed concept and to get the optimal results, there are no ESD protection structures for these pads. If the ESD protection circuit is used, it can be modeled in first order as a grounded capacitor parallel with the bonding wire inductor. The parallel LC network should be used to replace the L_{add} in the analysis used in this paper.

The proposed LNA topology shown in Fig. 4 is designed with TSMC 0.35 μm CMOS technology and the noise performance is shown in Fig. 5. L_g is an ideal inductor, while L_s and L_d are on-chip spiral inductors, which are modeled as pi model using ASITIC software [15], [16].

The proposed technique reduces the differential cascode CS-LNA noise figure (NF) by 15.8%, that is from 2.22 dB to 1.87 dB at 2.2 GHz. It will be more significant for the LNAs working at higher frequency.

At the lower frequency, L_{add} short circuited the gates of the cascode transistors to V_{DD} supply (AC ground). In that case, the

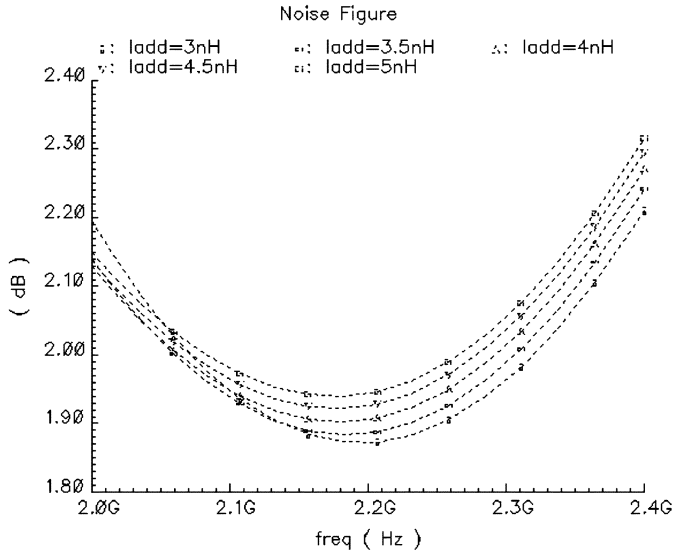


Fig. 6. Simulated NF of the differential cascode CS-LNA with the inductor L_{add} value varied from 3 to 5 nH.

total capacitive effects at node X in Fig. 4 are not zero and the LNA has worse noise performance.

The bonding wire inductance has different PVT values. From (10)–(14), at the operating frequency, we obtain that the variations of $G'_{m,eff}$, B'_{eff} and F' can be approximated as

$$\Delta G'_{m,eff} = G'_{m,eff}(L_{add} + \Delta L_{add}) - G'_{m,eff}(L_{add}) \cong 0 \quad (15)$$

$$\Delta B'_{eff} = B'_{eff}(L_{add} + \Delta L_{add}) - B'_{eff}(L_{add}) \cong \frac{1}{\omega_o L_{add}} \times \frac{\Delta L_{add}}{L_{add}} \quad (16)$$

$$\begin{aligned} \Delta F' &= F'(L_{add} + \Delta L_{add}) - F'(L_{add}) \\ &\cong 4R_s \gamma_2 g_{d02} \left(\frac{\omega_o \Delta B'_{eff}}{\omega_T G'_{m,eff}} \right)^2 \\ &= 4R_s \gamma_2 g_{d02} \left(\frac{\omega_o (4C_{gs2} + C_{sb2} + C_{gd1} + C_{db1})}{\omega_T G'_{m,eff}} \right)^2 \\ &\quad \times \left(\frac{\Delta L_{add}}{L_{add}} \right)^2. \end{aligned} \quad (17)$$

From (15)–(17), as an example, with 10% variation in L_{add} value, the proposed technique can still achieve around 96% noise reduction for the cascode device, assuming the ideal L_{add} can entirely eliminate the cascode transistor noise contribution. The noise performance of the LNA with varied inductor L_{add} value (from 3 nH to 5 nH) is shown in Fig. 6. The NF varied from 1.87 dB to 1.95 dB, that is 4.2% variation for a 67% variation of L_{add} .

The LNA NF varies with temperature. The noise reduction with the proposed technique through temperature variation is summarized in Table I. Since the noise of the transistor increases with the increasing temperature, the absolute value of the cascode transistor noise contribution also increases. Thus, if it is ideally eliminated, the absolute noise reduction value becomes larger at higher temperature.

TABLE I
NF IMPROVEMENT VERSUS TEMPERATURE

		-45°C	27°C	85°C
NF	without proposed technique	1.59dB	2.22dB	3.22dB
NF	with proposed technique	1.42dB	1.87dB	2.4dB
NF	improvement	0.17dB	0.35dB	0.82dB

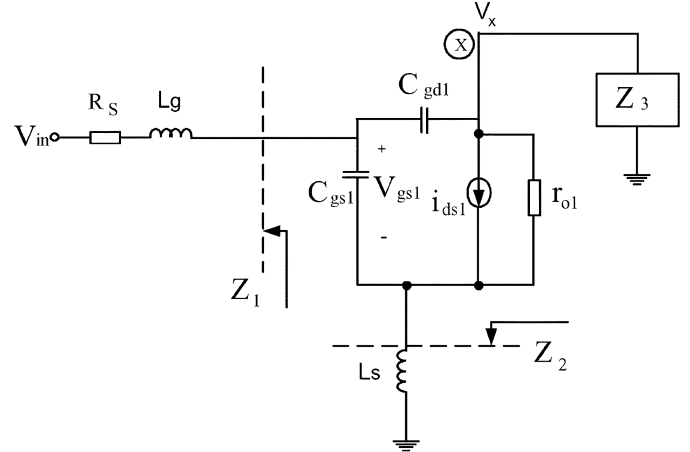


Fig. 7. Analyzed CS stage of cascode CS-LNA equivalent circuit.

IV. LNA LINEARITY IMPROVEMENT WITH THE PROPOSED TECHNIQUE

The LNA linearity is normally dominated by the voltage to current conversion transistor in CS stage. If the voltage gain of the first stage is greater than one, the second stage linearity plays a more important role [14]. Since the cascode CS-LNA can be treated as a CS-CG two stage amplifier, the linearity of the proposed topology is analyzed in two parts: 1) the linearity of the first voltage to current conversion stage; 2) the linearity of the cascode stage.

The linearity of the common source MOS transistor or common emitter bipolar transistor is well reported in the literature [17]–[22]. The linearity of the first voltage to current conversion stage is analyzed based on Fig. 7.

The drain currents of M1 and M2 in Fig. 4 can be expressed as follows up to third order:

$$i_{ds} \approx I_{DC} + g_m V_{gs} + g_2 V_{gs}^2 + g_3 V_{gs}^3. \quad (18)$$

The third-order input intercept point (IIP3) of the first voltage to current conversion stage can be derived using Volterra series [17]–[19] as shown in (19)–(23):

$$\text{IIP}_3 = \frac{1}{6R_s \cdot |H(\omega)| \cdot |A_1(\omega)|^3 \cdot |\varepsilon(\Delta\omega, 2\omega)|} \quad (19)$$

$$\varepsilon(\Delta\omega, 2\omega) = g_3 - g_{oB} \quad (20)$$

$$g_{oB} = \frac{2}{3} g_2^2 \left[\frac{2}{g_{m1} + g(\Delta\omega)} + \frac{1}{g_{m1} + g(2\omega)} \right] \quad (21)$$

$$g(\omega) = \frac{1 + j\omega C_{gd}[Z_1(\omega) + Z_3(\omega)] + j\omega C_{gs}[Z_1(\omega) + Z_x(\omega)]}{Z_x(\omega)} \quad (22)$$

$$Z_x(\omega) = Z_2(\omega) + j\omega C_{gd}[Z_1(\omega)Z_2(\omega) + Z_1(\omega)Z_3(\omega) + Z_2(\omega)Z_3(\omega)] \quad (23)$$

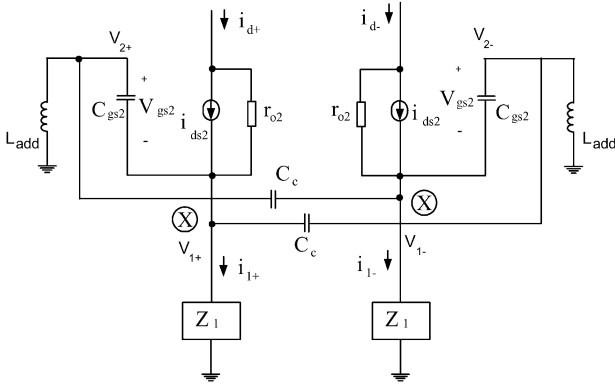


Fig. 8. Analyzed cascode stage equivalent circuit.

where ω is the center frequency of two input tones: ω_1 and ω_2 , $\Delta\omega = |\omega_1 - \omega_2|$, $|H(\omega)|$ relates the equivalent input IM3 voltage to the IM3 response of the drain current nonlinear terms, $A_1(\omega)$ is the linear transfer function from the input voltage V_{in} to the gate-source voltage V_{gs1} . $Z_1(\omega)$ and $Z_2(\omega)$ are shown in Fig. 4. $\varepsilon(\Delta\omega, 2\omega)$ shows the nonlinear contributions from the second and third order terms described in (18). For a MOS transistor, it can be found that g_3 and g_{oB} have opposite signs. From (19)–(20), the reduction of both g_3 and g_{oB} is needed to improve the IIP3.

Z_3 is the impedance looking out of the drain of the main transistor M_1 . For the conventional cascode CS-LNA [1]–[4], its relation with the cascode transistor M_2 is described as

$$Z_3(\Delta\omega) \approx \frac{1}{g_{m2}} \quad (24)$$

$$Z_3(2\omega) \approx \frac{1}{g_{m2} + j2\omega C_{gs2}}. \quad (25)$$

From (10)–(11), for our proposed LNA, the above values become

$$Z'_3(\Delta\omega) = \frac{1}{G'_{m,\text{eff}}(\Delta\omega) + jB'_{\text{eff}}(\Delta\omega)} \approx \frac{1}{g_{m2}} \quad (26)$$

$$\begin{aligned} Z'_3(2\omega) &= \frac{1}{G'_{m,\text{eff}}(2\omega) + jB'_{\text{eff}}(2\omega)} \\ &\approx \frac{1}{2g_{m2} + j8\omega C_{gs2}}. \end{aligned} \quad (27)$$

Z_3 is the same at $\Delta\omega$, and is smaller at 2ω for the proposed LNA. From (19)–(27), we can find that the proposed LNA reduces the load impedance (Z_3) of the main transistor M_1 and therefore reduces g_{oB} and $\varepsilon(\Delta\omega, 2\omega)$, resulting in a higher IIP3.

The linearity of the cascode stage is next analyzed based on Fig. 8, where currents $i_{ds2} = g_{m2}(V_2 - V_x)$, i_{1+} and i_{1-} are the differential input signals and i_{d+} and i_{d-} are the differential output signals.

For the cascode stage without the proposed technique, we can express i_d as

$$i_d = i_1 - g(\omega) \cdot V_{gs2} \quad (28)$$

where i_1 is the differential input current ($i_{1+} - i_{1-}$), i_d is the differential output current ($i_{d+} - i_{d-}$), V_{gs2} is the gate-source

voltage of the cascode transistor, and

$$g(\omega) = j\omega C_{gs2}. \quad (29)$$

From (28)–(29), due to C_{gs2} , the nonlinearity of transistor M_2 influences the overall linearity of the LNA. The A_{IIP3} of the conventional cascode stage without L_{add} and C_c can be derived using Volterra series as

$$A_{\text{IIP3}}^2 = \frac{4}{3} \cdot \frac{1}{|H(\omega)| \cdot |A_1(\omega)|^3 \cdot |\varepsilon(\Delta\omega, 2\omega)|}. \quad (30)$$

$\varepsilon(\Delta\omega, 2\omega)$ and g_{oB} are defined the same as in (20) and (21):

$$H(\omega) = \frac{g(\omega)}{g_{m1}} \quad (31)$$

$$A_1(\omega) = \frac{1}{g_{m1} + g(\omega)}. \quad (32)$$

For the cascode stage with the proposed technique, we can obtain

$$i_d = i_1 - g'(\omega) \cdot V_{gs2} \quad (33)$$

$$\begin{aligned} g'(\omega) &= \frac{4j\omega C_{gs2} \cdot j\omega C_c + \frac{1}{j\omega L_{\text{add}}}(j\omega C_{gs2} + j\omega C_c)}{2j\omega C_c + \frac{1}{j\omega L_{\text{add}}}} \\ &\quad + \omega C_{sb2} + \omega C_{gd1} + \omega C_{db1}. \end{aligned} \quad (34)$$

Note that in (33), the current flowing into C_c is included. If $\omega C_c \gg \omega C_{gs2}$, $\omega C_c \gg \omega C_{gs2} - (1/\omega L_{\text{add}})$ and inductor L_{add} resonates with the effective capacitance at node X at $\omega = \omega_o$, (34) becomes

$$g'(\omega) \approx \frac{1}{j\omega_o L_{\text{add}}} + 4j\omega_o C_{gs2} + \omega_o C_{sb2} + \omega_o C_{gd1} + \omega_o C_{db1} \approx 0 \quad (35)$$

and (33) yields

$$i_d = i_1 - g'(\omega_o) \cdot V_{gs2} \approx i_1. \quad (36)$$

Thus, according to (36), there is no linearity degradation from the cascode stage.

The A_{IIP3} of the cascode stage with the proposed technique has the same expression as (30) but with different $g(\omega)$ as defined by (34). From the simulation, the proposed technique increases the linearity by 2.35 dBm as shown in Fig. 9.

From (33)–(36), the inductor L_{add} can resonate with the effective capacitance at node X to completely remove the nonlinearity contribution from the cascode transistor M_2 . The linearity improvement will vary with different L_{add} values due to the PVT variation. The IIP3 of LNA is shown in Table II. It varied less than 1.2 dBm with inductor value varied from 0% to 10%.

For the proposed cascode LNA topology shown in Fig. 4, we can draw the conclusion that the capacitive cross-coupling technique improves the linearity by increasing the effective transconductance of the cascode stage (M_2), thus reducing the load impedance of the main transistor M_1 . Therefore, the reduced voltage swing at node X (drain of M_1) improves the linearity of CS stage of the LNA. The inductor L_{add} resonates

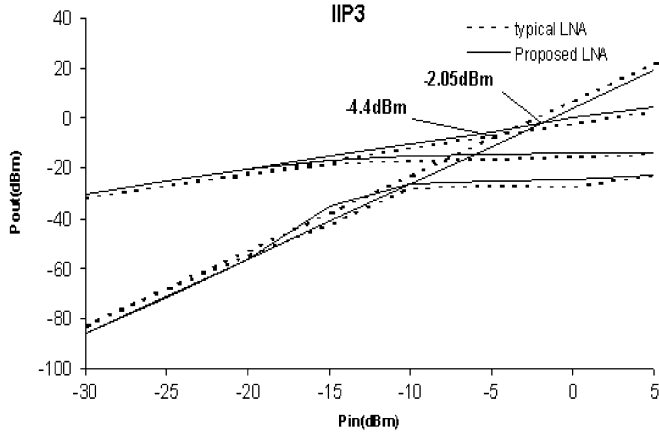


Fig. 9. IIP3 of the differential cascode CS-LNA with and without L_{add} and C_c .

TABLE II
IIP3 VERSUS L_{add}

	Typical LNA	Proposed LNA with varied L_{add}		
		3nH (0%)	3.15nH (5%)	3.3nH (10%)
IIP3(dBm)	-4.4	-2.05	-2.3	-2.5

with the parasitic capacitance at node X and therefore eliminates the nonlinearity and noise contribution from the cascode stage.

V. EFFECTS OF THE TECHNIQUE ON THE LNA S11, VOLTAGE GAIN, AND LNA STABILITY

A. Effect on the LNA S11

For the typical cascode CS-LNA, C_{gd1} of the transistor M_1 reflects Miller impedance at the gate of M_1 . However, it is not purely capacitive and its susceptance yields

$$\begin{aligned}
 B_{\text{mill1}}(j\omega) &= (1 + A_v(j\omega)) \times sC_{gd1} \\
 &= \frac{j\omega C_{gd1} g_{m1}}{1 + j\omega g_{m1} \frac{L_s}{C_{gs1}} - L_s C_{gs1}} \\
 &\quad \times \frac{1}{g_{m2} + j\omega C_x} \quad (37)
 \end{aligned}$$

where $A_v(j\omega)$ is the voltage gain from the gate to the drain of M_1 , and C_x is defined in (2). For the proposed LNA, it changes to

$$\begin{aligned}
 B'_{\text{mill1}}(j\omega) &= (1 + A_v'(j\omega)) \times sC_{gd1} \\
 &= \frac{j\omega C_{gd1} g_{m1}}{1 + j\omega g_{m1} \frac{L_s}{C_{gs1}} - L_s C_{gs1}} \\
 &\quad \times \frac{1}{G'_{m,\text{eff}} + jB'_{\text{eff}}} \quad (38)
 \end{aligned}$$

where $G'_{m,\text{eff}}$ and B'_{eff} are defined in (10)–(12). According to (37)–(38), since the effective transconductance of the cascode stage increases, the gain of the first stage reduces, which leads to a reduced Miller effect of C_{gd1} of transistor M_1 . Therefore, the

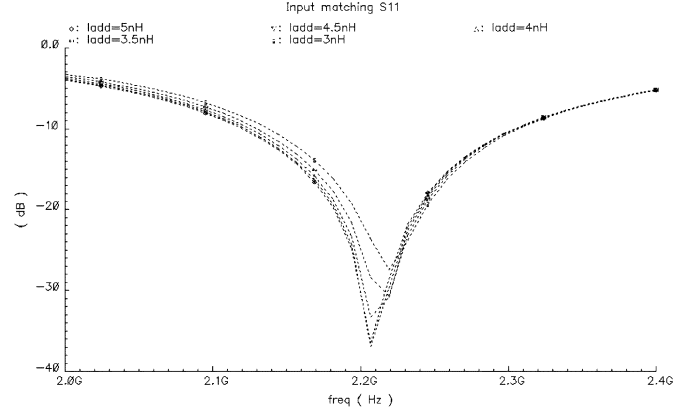


Fig. 10. Simulated S11 of the differential cascode CS-LNA with the inductor L_{add} value varied from 3 nH to 5 nH.

input matching is not very sensitive to the variations of the inductor L_{add} . According to Fig. 10, the input resonant frequency varied less than 1% for the L_{add} value varied 66%, which is from 3 nH to 5 nH.

B. Effect on the LNA Voltage Gain

Under the input impedance matched condition, the voltage gain of the inductively degenerated cascode CS-LNA can be derived from Figs. 1 and 2.

$$\begin{aligned}
 A_v(j\omega) &= g_{m1} \frac{1}{2R_s \omega_o C_{gs1}} \frac{g_{m2}}{\sqrt{(g_{m2})^2 + (\omega_o C_x)^2}} Z_o \\
 &= g_{m1} Q_{\text{in}} Z_o \frac{g_{m2}}{\sqrt{(g_{m2})^2 + (\omega_o C_x)^2}} \quad (39)
 \end{aligned}$$

where $Q_{\text{in}} = 1/2R_s \omega_o C_{gs1}$ is the quality factor of the LNA input network and Z_o is the overall output impedance. With the proposed technique, the cascode CS-LNA gain of Fig. 4 becomes

$$A_v(j\omega) = g_{m1} Q_{\text{in}} Z_o \frac{G'_{m,\text{eff}}}{\sqrt{(G'_{m,\text{eff}})^2 + (B'_{\text{eff}})^2}} \quad (40)$$

$G'_{m,\text{eff}}$ and B'_{eff} are defined in (10)–(12).

The gain of the designed fully differential CS-LNA is shown in Fig. 11, where the LNA drives a 50 Ω resistor. According to (39)–(40) and simulation results in Fig. 11, the proposed technique increases the overall LNA gain by around 2 dB.

In most of the wireless transceivers, the following stage of the LNA is a mixer. It is a capacitive load rather than a 50 Ω load, which is the case in this simulation. The source-follower can drive the off-chip 50 Ω with the voltage gain around 1. A source-follower buffer is added after the LNA to drive a 50 Ω load. This testing setup of the LNA voltage gain is shown in Fig. 12 where LNA drives a buffer. Fig. 13 is the simulated LNA voltage gain. The LNA is simulated with a source-follower to drive the off-chip 50 Ω and the voltage gain of interest is investigated before the source-follower. We used an ideal balun in the simulation. In practice, the LNA directly drives a practical balun without the source-follower buffer. The noise and gain influence of the balun is de-embedded. In this way, we can estimate the LNA

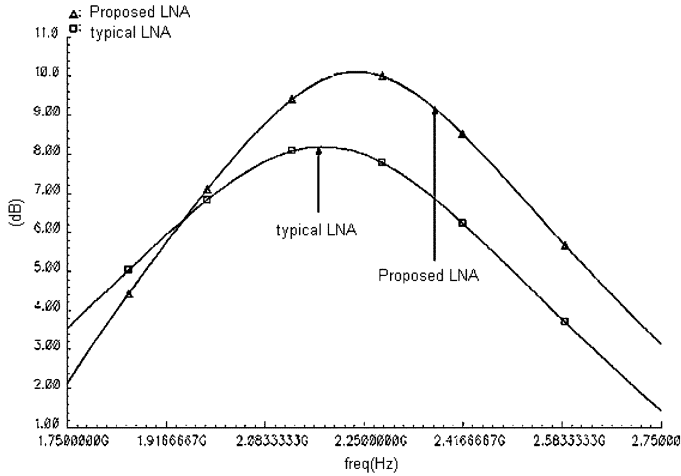


Fig. 11. Voltage gain simulation results of the fully differential cascode CS-LNA with and without L_{add} and C_c .

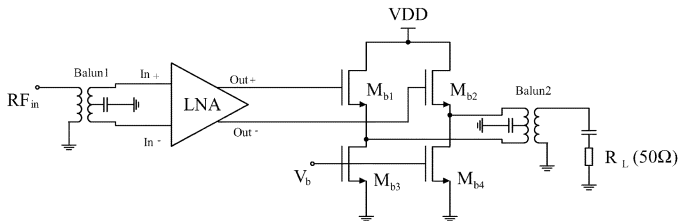


Fig. 12. Voltage gain testing setup of the fully differential cascode CS-LNA when driving the on-chip buffer.

voltage gain while driving the mixer in the wireless receiver. Since the buffer provides a 250 fF capacitive load rather than a 50 Ω resistive load, the LNA voltage gain increases to 20.4 dB as shown in Fig. 13.

C. Effect on the LNA Stability

The stability factor [4] of the LNA is defined as

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \quad (41)$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$.

The unconditional stability requirement of LNA is $K > 1$ and $|\Delta| < 1$. When the input and output of the LNA are matched to the source and load impedance, S_{11} and S_{22} are almost 0. With the decreasing of S_{12} , $|\Delta|$ reduces, which means better stability of the LNA. The S_{12} reflects the input–output isolation of the LNA. Compared with the typical LNA, the added inductor L_{add} at the gate of the cascode transistor M2 along with the inherent capacitances provides a low impedance path for the output signal feedback to the input, which helps to improve the input–output isolation (S_{12}) [23]. The cross-coupling capacitor C_c forms a signal path from the gate of the cascode transistor M2 to the source of M2, which reduces the isolation effect of the transistor M2. The proposed technique presents an overall comparable isolation effect with the typical LNA with around 3 dB worse S_{12} value in the simulation. From simulation, the K value of the LNA is 52.5 at 2.2 GHz without L_{add} and C_c . K becomes 30.5 at 2.2 GHz with L_{add} and C_c . The difference of the K value is partly due to the 2 dB S_{21} difference and 3 dB S_{12} difference with/without L_{add} and C_c . The LNA is stable in both cases.

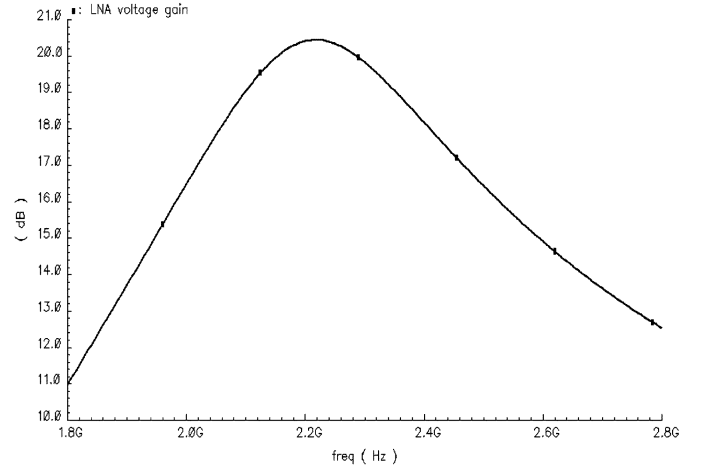


Fig. 13. Voltage gain simulation results of the fully differential cascode CS-LNA when driving an on-chip buffer.

VI. DESIGN AND MEASUREMENT RESULTS

A fully differential cascode CS-LNA was designed and fabricated using a proposed inclusive noise reduction and linearity improvement technique. The inductor L_g is an off-chip inductor. The added inductor L_{add} (around 3 nH) is a bonding wire inductor. The inductors L_s (0.5 nH) and L_d (3 nH) are on-chip spiral inductors, with $Q \approx 3$. The design was implemented using TSMC 0.35 μm CMOS technology. The chip microphotograph is shown in Fig. 14. The LNA occupies 1300 $\mu\text{m} \times 1000 \mu\text{m}$ active area, with the LNA core using 850 $\mu\text{m} \times 850 \mu\text{m}$ active area.

L_g value is adjusted in the measurement to achieve the input impedance matching at the desired frequency. Fig. 15 shows the measured S_{11} , S_{21} , and S_{12} . The LNA power gain is 8.4 dB at 2.2 GHz. If followed by a buffer, the LNA output impedance is larger than 50 Ω and the LNA gain increases up to 20.4 dB in simulation. S_{11} is less than -13 dB, and S_{12} is less than -30 dB. Fig. 16 shows the measured NF of the LNA. The LNA has 1.92 dB NF. The IIP3 was measured using a two-tone test: 2.2 GHz and 2.22 GHz. It is shown in Fig. 17. The IIP3 is -2.55 dBm. The core LNA draws 9 mA from a 1.8 V power supply. Due to the mismatch of the gate inductor L_{add} , the noise of the power supply can inject into the LNA output. The power supply rejection ratio (PSRR) of the LNA with 5% and 10% L_{add} mismatches is shown in Fig. 18. The LNA has better than -24 dB PSRR at 2.2 GHz with 10% L_{add} mismatch.

The comparison of this LNA with the published literatures is summarized in Table III. Although the designed LNA is a fully differential structure in 0.35 μm process, it provides the best noise performance. The published LNAs consume less bias current because of the single-ended structure and more advanced technology. The linearity in [24] is higher due to the larger bias current and more voltage headroom for the transistors. Although the current source of the designed fully differential LNA reduces the voltage headroom, it still achieves comparable linearity with respect to [25]. The LNA gain is proportional to the inductor quality factor and the inductor value as shown below [25]:

$$\text{Gain} \propto R_p \propto Q_d^2 R_d \propto \omega_o Q_d L_d \quad (42)$$

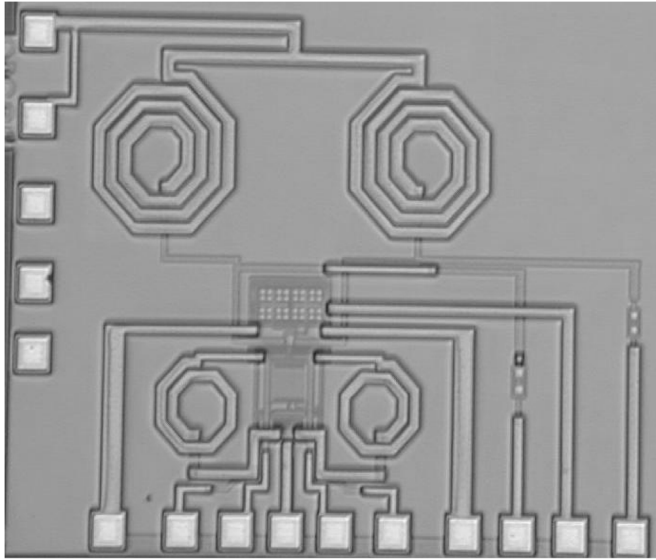


Fig. 14. Chip micrograph of the differential cascode CS-LNA.

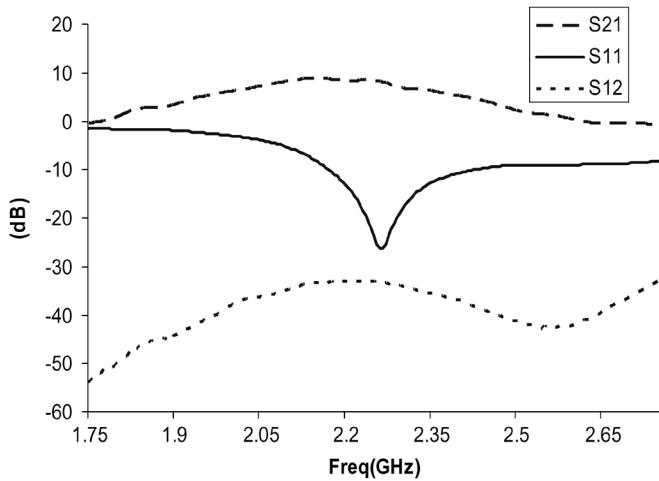


Fig. 15. Measured S11, S12 and S21 of the differential cascode CS-LNA.

where R_d is the series resistance of L_d , R_p is the parallel resistance of L_d obtained from the series to parallel transformation, and Q_d is the quality factor of L_d . The LNA is designed in $0.35 \mu\text{m}$ process with a low Q on-chip inductor, which results in a smaller gain. After adding a buffer (with similar input impedance of a typical CMOS Gilbert cell) after the LNA, the LNA can achieve around 20.4 dB voltage gain, which is sufficient for a number of wireless applications.

In the deep-submicron process, the parasitic capacitance of the devices is smaller, thus its effect explained in this paper becomes less significant at the lower operating frequency, but as the operating frequency increases to such as 10 GHz or higher, the same effect will appear even in the advanced process. On the other hand, the output impedance of the transistor is smaller in the advanced process, which increases the noise contribution of the cascode transistor. This effect combined with the parasitic capacitance makes the cascode transistor to be still an important noise contributor. The proposed technique can still be effective under these conditions, and the theoretical analysis is also valid. The proposed solution applies the capacitive cross-coupling technique to the cascode transistor of the LNA,

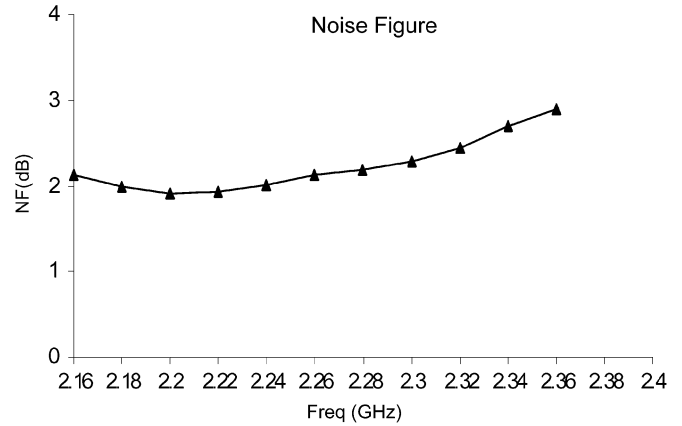


Fig. 16. Measured NF of the differential cascode CS-LNA.

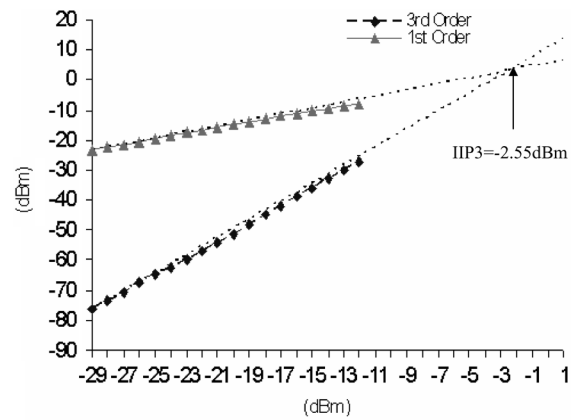


Fig. 17. Measured IIP3 of the differential cascode CS-LNA, with two tones at 2.2 GHz and 2.22 GHz.

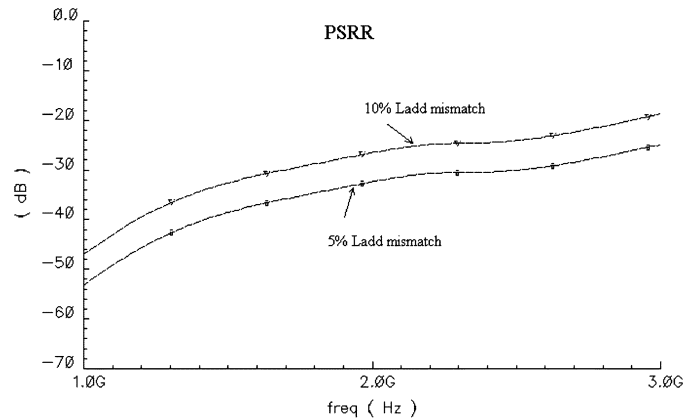


Fig. 18. PSRR of the LNA with 5% and 10% L_{add} mismatches.

which can increase the effective transconductance of the cascode transistor and improve the linearity of the common source stage of the LNA. The gate inductor effectively combined with the cross-coupling capacitor can reduce the noise and the non-linearity influence of the cascode transistor with a smaller inductor value as proved in Sections III and IV. To verify our proposed technique in the deep-submicron process, the LNA is designed in UMC $0.13 \mu\text{m}$ CMOS process and simulated based on the noise model provided by UMC. At 10 GHz, the proposed technique reduces the differential cascode CS-LNA NF from 1.55 dB to 0.95 dB, with L_{add} value as 0.5 nH.

TABLE III
PERFORMANCES COMPARED WITH PRIOR PUBLISHED CASCODE CS-LNAs

Parameters	[24]	[25]	[26]	[27]	This work	
					Simulated	Measured
Frequency (GHz)	2.45	2.46	2.4	0.95	2.2	2.2
S11(dB)	<-14.2	<-18.4	<-33	<-14	<-13	<-13
S21(dB)	15.1*	14	6	17	10 (20.4) [†]	8.6
NF(dB)	2.88	2.36	4.8	3.4	1.87	1.92
IIP3 (dBm)	2.2	-2.2	0.55	-5.1	-2.05	-2.55
Bias current (mA)	8.1	3.1	N/A	5.6	4.5×2	4.5×2
Power supply(V)	3	1.5	3.3	2.3	1.8	1.8
Topology	Single-ended	Single-ended	Single-ended	Single-ended	Fully-differential	Fully-differential
CMOS Process	0.25μm	0.15μm	0.35μm	0.35μm	0.35μm	0.35μm

*: In fact in [24] they reported the transducer gain.

†: 20.4 dB is obtained when an output buffer is used instead of 50Ω load.

VII. CONCLUSION

In this paper, a noise reduction and linearity improvement technique for a differential cascode CS-LNA was proposed. The inductor connected at the gate of the cascode transistor and the capacitive cross-coupling are strategically combined to reduce the noise and nonlinearity contributions of the cascode transistors. It is the first time that the capacitive cross-coupling technique is applied to the cascode transistors of the CS-LNA. It increases the effective transconductance of the cascode transistor, reduces the impedance seen out by the drain of the main transistor, and thus improving the linearity of the CS stage in the LNA. The inductor L_{add} resonates with the effective capacitance at the drain node of the main transistor with smaller inductance value compared with the typical inductor based technique. It ideally removes the noise and linearity influences from the cascode transistor, and results in a higher voltage gain. The proposed technique is theoretically formulated. From simulation results in TSMC 0.35 μm CMOS process, it reduces the LNA NF by 0.35 dB at 2.2 GHz, and improves the LNA IIP3 by 2.35 dBm. To illustrate the use of the proposed approach in small-size technology, a 10 GHz LNA is also designed using UMC 0.13 μm CMOS process. The proposed technique reduces the NF from 1.55 dB to 0.95 dB, which is simulated based on the noise model provided by UMC. This verifies the validity of our proposed technique in the deep-submicron process.

APPENDIX A

NOISE ANALYSIS OF THE PROPOSED LNA

For the typical CS-LNA in Fig. 1, the noise factor can be calculated using the small-signal model in Fig. 2. Following the procedure in [1]–[4], when ignoring the cascode transistor, the noise factor of the CS LNA is derived as

$$F_1 = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha} \frac{\chi}{Q_L} \frac{\omega_o}{\omega_T} \quad (\text{A.1})$$

where χ and Q_L are defined in (5)–(6).

Due to the existence of the parasitic capacitance C_x in Figs. 1 and 2, the noise factor of the CS-LNA is influenced by the cascode transistor M_2 .

The drain noise current of the cascode transistor M_2 is

$$\overline{i_{d2}^2} = 4KT\gamma_2 g_{do2} \Delta f. \quad (\text{A.2})$$

The input-referred noise at the source of the cascode transistor is

$$\overline{V_{n,d2}^2} = \overline{i_{d2}^2} \times \left(\frac{\omega_o C_x}{(\omega_o C_x + g_{m2})g_{m2}} \right)^2. \quad (\text{A.3})$$

The voltage gain from the input to the source of the cascode transistor is

$$A_{v1} = \frac{g_{m1}}{2\omega_o C_{gs1} R_s} \times \frac{1}{\omega_o C_x + g_{m2}}. \quad (\text{A.4})$$

The CS-LNA can be treated as a CS-CG two stage amplifier. Following the cascode network noise calculation theory [4], the noise factor of the CS-LNA is derived as

$$F = F_1 + \frac{\overline{V_{n,d2}^2}}{\overline{V_{n,Rs}^2} (A_{v1})^2} = F_1 + \frac{\overline{V_{n,d2}^2}}{4KTR_s (A_{v1})^2}. \quad (\text{A.5})$$

Substituting (A.2), (A.3), and (A.4) into (A.5), we can get

$$F = F_1 + F_c = F_1 + 4R_s \gamma_2 g_{do2} \left(\frac{\omega_o^2 C_x}{\omega_T g_{m2}} \right)^2. \quad (\text{A.6})$$

The C_x plays an important role in the LNA noise performance especially at the higher frequency.

After applying the proposed technique, the cascode transistor provides an equivalent transconductance, $G'_{m,\text{eff}}$, and susceptance, B'_{eff} .

$$F' = F_1 + F'_c = F_1 + 4R_s \gamma_2 g_{do2} \left(\frac{\omega_o B'_{\text{eff}}}{\omega_T G'_{m,\text{eff}}} \right)^2 \quad (\text{A.7})$$

where $G'_{m,\text{eff}}$ and B'_{eff} are defined in (10) and (11).

By reducing the value of $(B'_{\text{eff}}/G'_{m,\text{eff}})$, the LNA can obtain better noise performance.

Applying KCL to every node of the model in Fig. 8,

$$SC_{gs2}(V_{2+} - V_{1+}) + i_{d+} + SC_c(V_{2-} - V_{1+}) = i_{1+} \quad (\text{B.20})$$

$$SC_c(V_{1-} - V_{2+}) = SC_{gs2}(V_{2+} - V_{1+}) + sL_{\text{add}}V_{2+} \quad (\text{B.21})$$

$$V_{1-} = -V_{1+} \quad (\text{B.22})$$

$$V_{2-} = -V_{2+} \quad (\text{B.23})$$

$$i_{1-} = -i_{1+} \quad (\text{B.24})$$

$$i_{d-} = -i_{d+}. \quad (\text{B.25})$$

For the cascode stage with the proposed technique, we can get

$$i_d = i_1 - g'(\omega) \cdot V_{gs2} \quad (\text{B.26})$$

$$g'(\omega) = \frac{4j\omega C_{gs2} \cdot j\omega C_c + \frac{1}{j\omega L_{\text{add}}}(j\omega C_{gs2} + j\omega C_c)}{2j\omega C_c + \frac{1}{j\omega L_{\text{add}}}} + \omega C_{sb2} + \omega C_{gd1} + \omega C_{db1}. \quad (\text{B.27})$$

Replacing (B.16) with (B.27), all the other results from (B.15)–(B.19) are still valid.

For the proposed technique, if (B.27) equals zero, the current generated by M_1 will all flow to the output without nonlinearity degradation. This helps to improve the LNA linearity.

For the typical CS-LNA with a cascode transistor, the nonlinearity degradation can be evaluated by (B.15). From DC simulation, calculate the gate source capacitance C_{gs2} , the first order transconductance g_m , the second order nonlinearity term g_2 and the third order nonlinearity term g_3 . Calculate $g(\omega)$, g_{oB} , $\varepsilon(\Delta\omega, 2\omega)$ and $H(\omega)$ using (B.16)–(B.19). Calculate the input third order intermodulation using (B.15).

APPENDIX C

VOLTAGE GAIN AND S11 ANALYSIS OF THE PROPOSED LNA

From Fig. 1 and 2, the voltage gain from the input to the source of the cascode transistor is

$$A_{v1} = g_{m1}Q_{\text{in}1} \times \frac{1}{\omega_o C_x + g_{m2}} = \frac{g_{m1}}{2\omega_o C_{gs1}R_s} \times \frac{1}{\omega C_x + g_{m2}}. \quad (\text{C.1})$$

The voltage gain of the cascode stage is

$$A_{v2} = g_{m2}Z_o. \quad (\text{C.2})$$

The overall voltage gain of the LNA is now calculated as

$$A_v = A_{v1} \times A_{v2} = \frac{g_{m1}}{2\omega_o C_{gs1}R_s} \times \frac{g_{m2}}{\omega C_x + g_{m2}} Z_o. \quad (\text{C.3})$$

The magnitude of the overall voltage gain is calculated as in (39).

After applying the proposed technique, the cascode transistor provides an equivalent transconductance, $G'_{m,\text{eff}}$, and susceptance, B'_{eff} .

$$A_v = \frac{g_{m1}}{2\omega_o C_{gs1}R_s} \times \frac{G'_{m,\text{eff}}}{B'_{\text{eff}} + G'_{m,\text{eff}}} Z_o \quad (\text{C.4})$$

where $G'_{m,\text{eff}}$ and B'_{eff} are defined in (10) and (11).

From Fig. 1, when ignoring the Miller effect of the C_{gd1} , the voltage gain from the gate of M1 to the source of the cascode transistor is calculated as

$$A_{v,g} = \frac{\frac{g_{m1}}{sC_{gs}}}{g_{m1}\frac{L_s}{C_{gs}} + sL_s + \frac{1}{sC_{gs}}} \frac{1}{\omega C_x + g_{m2}}. \quad (\text{C.5})$$

The gate-drain capacitor is a Miller capacitor across the gate and the drain of the M1. The equivalent Miller susceptance at the gate of M1 is calculated as

$$B_{\text{mill1}}(j\omega) = (1 + A_{v,g}(j\omega)) \times sC_{gd1}. \quad (\text{C.6})$$

Substituting (C.5) into (C.6), we can get (37).

After applying the proposed technique, the cascode transistor provides an equivalent transconductance, $G'_{m,\text{eff}}$, and susceptance, B'_{eff} . The Miller susceptance (37) becomes (38).

ACKNOWLEDGMENT

The authors thank C. Mishra, M. Onabajo, S. Ganesan, Dr. C. Xin, W. Huang, M. El-Nozahi, and F. Abdel-Latif Hussien for helpful discussions. They would also like to thank X. Guan and R. Xu for their help in the chip measurement.

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