

An Injection-Locked Frequency Divider With Multiple Highly Nonlinear Injection Stages and Large Division Ratios

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Abstract—An injection-locked frequency divider (ILFD) with multiple highly nonlinear injection stages is discussed. Implemented in a standard 0.18- μm CMOS technology, measurement shows that multiple division ratios from 6 to 18 are achieved while the locking ranges are all above 1.7 GHz without the need for additional tuning. The ILFD can be locked at the maximum injection frequency of 11 GHz with the power consumption no more than 7.2 mW from a 1.8-V power supply.

Index Terms—Division ratio, injection locked frequency dividers (ILFDs), locking range.

I. INTRODUCTION

FREQUENCY dividers are widely used in phase-locked loops (PLLs) to divide down high-frequency voltage-controlled oscillator (VCO) output for comparison with the low-frequency external reference clock. Digital static frequency dividers are usually employed in conventional implementations, whose limitation on power consumption and maximum operating frequency drives IC designers to seek alternative solutions. One such candidate is the injection-locked frequency divider (ILFD).

ILFDs consist of free running oscillators synchronized to injected signals. They can be classified as *LC* oscillator based ILFDs (*LC*-ILFDs) and ring oscillator based ILFDs (ring-ILFDs). The high quality factor Q and narrow band nature of *LC* oscillators limit the locking range of an *LC*-ILFD. Its locking range would likely fail to cover the desired operating range in the presence of process parameter variations. To maximize the locking range, the Q of the *LC* tank can be lowered at the cost of either large die area [1] or high power consumption [2]. Although varactors can be used to increase the locking range [2], simultaneous tuning of the divider and the VCO in PLL is still a challenging problem. Another issue associated with *LC*-ILFD is that the output amplitude changes a lot along the locking range because the tank impedance drops rapidly when the output frequency is shifted from the resonant frequency. Power-hungry buffers have to be used to provide enough voltage swing for the robust operation of the circuitries following the ILFDs.

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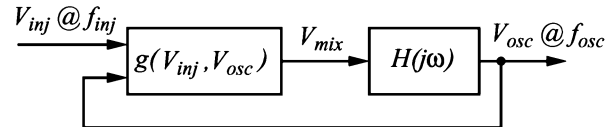


Fig. 1. Conventional model for ILFD [9].

With their low Q by nature, ring-ILFDs recently draw much research effort. They have larger locking ranges and less amplitude fluctuations [3]–[8]. However, although both *LC*-ILFDs and ring-ILFDs could work at very high frequencies, none of the existing solutions could provide large division ratios with acceptable locking ranges. Large division ratio is necessary to reduce the output frequencies of the ILFDs, which relaxes the requirements on speed and power for the following stages.

In this paper, a new architecture of ring-ILFD is presented. Although only three stages are used for the implementation in a standard 0.18- μm CMOS technology, the measurement results show that the division ratio can be as high as 6, 12, and 18 depending on the injection frequency. The corresponding locking ranges are 2.1, 1.9, and 1.7 GHz, respectively. The locking ranges are relatively large due to the multiple injection stages and highly nonlinear operation of the topology. The injection frequency could be up to 11.2 GHz while the power consumption is 7.2 mW.

II. CIRCUIT ARCHITECTURE

A. Study of Conventional ILFD Model

Verma *et al.* [9] introduced a general model for the ILFD as shown in Fig. 1. It consists of a nonlinear gain block g and a linear filter $H(j\omega)$. The nonlinear block mixes the injection signal V_{inj} with the oscillator input signal V_{osc} , which is the feedback from the output of the linear filter. The linear filter $H(j\omega)$ rejects frequency components far from f_{osc} and provides necessary phase shift to sustain the oscillations.

The frequency components at the output of the block g could be expressed as $|mf_{osc} \pm nf_{inj}|$, where f_{inj} is the fundamental frequency of V_{inj} , m , and n are integers. Assuming weak injection [9], n could be 0 and 1 since the harmonics of injection frequency are ignored. When $n = 0$, the dc component of V_{inj} is multiplied by the fundamental component f_{osc} of V_{osc} . The resulting product is denoted as V_{mix_DC} . If the nonlinear function g is assumed to be memoryless [9], there is no phase shift from f_{osc} of V_{osc} to V_{mix_DC} . When $n = 1$, the fundamental

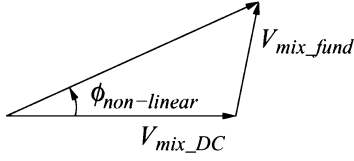


Fig. 2. Generation of $\phi_{\text{non-linear}}$ from $V_{\text{mix_DC}}$ and $V_{\text{mix_fund}}$.

component f_{inj} of V_{inj} is mixed with the harmonics of f_{osc} to generate a component at f_{osc} . The resulting product is denoted as $V_{\text{mix_fund}}$. For instance, for the division ratio of k between f_{inj} and f_{osc} ,

$$f_{\text{inj}} - (k - 1)f_{\text{osc}} = f_{\text{osc}} \implies f_{\text{osc}} = \frac{f_{\text{inj}}}{k}. \quad (1)$$

As the phase of f_{inj} relative to f_{osc} of V_{osc} is arbitrary, the phase of $V_{\text{mix_fund}}$ relative to $V_{\text{mix_DC}}$ is also arbitrary. Because the frequency component at f_{osc} in V_{mix} is the sum of $V_{\text{mix_DC}}$ and $V_{\text{mix_fund}}$, as shown in Fig. 2, the overall phase shift $\phi_{\text{non-linear}}$ depends on the relative amplitude and phase difference of these two components.

As suggested in [9], if the loop has sufficient gain so that the Barkhausen criterion of magnitude is satisfied, the locking range is determined by the phase criterion given by

$$\phi_{\text{linear}} + \phi_{\text{non-linear}} = 2i\pi \quad (2)$$

where ϕ_{linear} is the phase shift due to $H(j\omega)$ and i is an integer number. Since the value of ϕ_{linear} across frequencies is fixed for a certain ILFD, the ILFD fails to lock when the nonlinear block could not provide the required phase shift $\phi_{\text{non-linear}}$ to meet (2). The larger the range of $\phi_{\text{non-linear}}$, the larger the locking range is.

High nonlinearity increases the amplitude of $V_{\text{mix_fund}}$ so that it becomes more comparable to $V_{\text{mix_DC}}$. Therefore, more phase shift could be generated. As a result, not only the locking range for the small division ratio is extended, but the implementation of large division ratios is also made possible.

The range of $\phi_{\text{non-linear}}$ could also be enlarged by cascading multiple nonlinear stages in the circuit, under which case, the overall $\phi_{\text{non-linear}}$ consists of contributions of $\phi_{\text{non-linear}}$ from each stage. While it is difficult to have multiple injection stages in LC -ILFD, which normally consists of one-stage LC oscillator, ring-ILFD could provide multiple injection stages, which is usually realized with several identical stages in the loop.

B. Ring-ILFD With Multiple Highly Nonlinear Injection Stages

The above study of the general model of ILFDs shows that a large locking range could be achieved by implementing ring-ILFD with multiple highly nonlinear stages. The seeming disadvantage of using ring-ILFD is its poor internal phase noise. However, [9] shows that the internal stages' phase noise is high-pass filtered by the loop, which becomes negligible compared with the phase noise from the injection signal that is low-pass filtered. In addition, it is also shown that the pole frequency of the high-pass transfer function increases with the increase of the locking range. Therefore, one benefit of large locking range is that the contribution of internal phase noise to the output is much suppressed with a large frequency range.

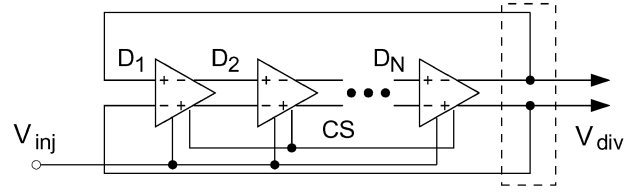


Fig. 3. Architecture of the proposed multiple highly nonlinear injection stage ring-ILFD.

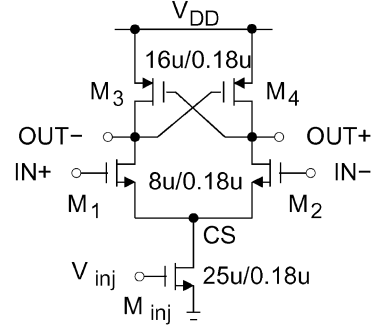


Fig. 4. Schematic of one stage of the proposed multiple highly nonlinear injection stage ring-ILFD.

The architecture of the proposed multiple highly nonlinear injection stage ring-ILFD is shown in Fig. 3. It consists of N stages of differential pair (M_{1-2}) with pMOS transistors (M_{3-4}) in positive feedback configuration as load, as shown in Fig. 4. If N is an even number, the outputs of the last stage need to be cross-coupled to the inputs of the first stage. The injection points are the gates of the current bias transistor M_{inj} in all stages. In this architecture, all stages share the common source node CS. The advantage of this approach is that the operating frequency of the ILFD is increased, which will be explained in the next section.

The high nonlinearity operation is achieved by using the positive feedback load. Similar technique was used in a saturated ring oscillator design [10]. By doing so, outputs with sharp transition and large amplitude are generated, both of which facilitate the nonlinearity. However, the strong nonlinear operation of the load transistors makes the conventional ILFD model not suitable for the analysis of the proposed ILFD. In the conventional model, the load is modeled as a linear block, which is not the case for the proposed ILFD. Without such linear blocks, the frequency domain analysis is not correct. Instead, large signal transient analysis has to be utilized.¹

III. LOCKING RANGE OF THE ILFD

A. Operation of the Free Running ILFD

Let us explain how one stage of the free running ILFD (Fig. 4) responds to a low-to-high transition at the input $\text{IN}+$ and a high-to-low transition at $\text{IN}-$. Before the transition, as both $V_{\text{in}+}$ and $V_{\text{out}+}$ are low, M_1 is OFF and M_3 is in the triode region. Meanwhile, M_2 is ON and M_4 is in the cut-off region as $V_{\text{in}-}$ and $V_{\text{out}-}$ are high. Right after this transition, M_1 turns

¹Similar method was introduced in [11], which was published during the review of this paper.

to the saturation region and provides a path for the current of M_{inj} to discharge the loading capacitance at V_{out-} . As M_3 is still in the triode region, the loading capacitance at $OUT-$ is only partially discharged by M_1 , where part of the current is absorbed by the low impedance of M_3 . Thus, the V_{out-} transition from high-to-low is slow at the beginning. In the meantime, as both M_2 and M_4 are in the cut-off region, V_{out+} does not change. This state continues until V_{out-} is below $V_{DD} - |V_{TP}|$ so that M_4 enters into the saturation region. Then M_4 provides current to charge the parasitic capacitance at $OUT+$. When V_{out+} increases, it in turn speeds up the discharging at $OUT-$ by increasing the output resistance of M_3 . A positive feedback is set up and the transitions at both outputs are then very fast. Therefore, the time delay from the input transition to the output transition is mainly determined by the variation of the output from V_{DD} to $(V_{DD} - |V_{TP}|)$, which is modeled as the drain current of M_{inj} discharging the parallel RC network formed by the loading capacitance and the low output resistance of the load transistor. If the common source node is not shared, the drain current of M_{inj} varies during the discharge. This is due to the fact that before the input transition, M_{inj} is pushed into the triode region as M_4 is in the cutoff region and M_2 is ON. Therefore, after the input transition, M_{inj} has to take time to change from the triode region to the saturation region, which effectively reduces the average discharging current available for the operation of the inverting stage. As a result, the output frequency decreases. For the common source node sharing topology, after the output transition at one stage, its following stage goes into transition mode, and sources the discharging drain current of M_{inj} . Therefore, M_{inj} stays in the saturation region, providing the constant current.

From the above discussion, the response of $V_{out-fr}(t)$ from V_{DD} to $V_{DD} - |V_{TP}|$ could be modeled as a constant current I_B discharging a RC parallel network. Hence, $V_{out-fr}(t)$ can be approximated as

$$V_{out-fr}(t) \approx V_{DD} - (1 - e^{-t/R_{out}C_{out}})I_B R_{out} U(t) \quad (3)$$

where $U(t)$ is the step function. The time delay, t_d , defined as the time that it takes for the output to be changed from V_{DD} to $V_{DD} - |V_{TP}|$, is computed as

$$t_{d-fr} \approx R_{out} C_{out} \ln \frac{1}{1 - |V_{TP}|/(I_B R_{out})} \quad (4)$$

where R_{out} is the output resistance of M_3 in triode region, C_{out} is the loading capacitance at $OUT-$, including the parasitic capacitance and the input capacitance of next stage. Thus, the free running oscillation frequency is approximately given by the following expression:

$$f_{osc-fr} \approx \frac{1}{2N t_{d-fr}} \quad (5)$$

where N is the number of stages in the ILFD.

B. Locking Range of the ILFD

We will first show that in the locked state, i.e., $f_{osc} = f_{inj}/2kN$, each stage sees the same time delays of its input signal and the injection signal. This conclusion provides the

basis for us to predict the locking condition by analyzing the operation of a single stage.

Let us consider two stages, stage J and $(J + P)$. Assume that the input of stage J is expressed as $V_{in,J}(t)$. Under the locked state, if t_{d-inj} is the delay of one stage, the input of stage $(J + P)$ is delayed from $V_{in,J}(t)$ by $P \cdot t_{d-osc}$, where $t_{d-osc} = 1/(2N f_{osc}) = k/f_{inj}$. Therefore, $V_{in,P}(t)$ could be expressed as $V_{in,J}(t - Pk/f_{inj})$. Meanwhile, for the injection signal $V_{inj}(t)$, due to its periodic nature, $V_{inj}(t - Pk/f_{inj}) = V_{inj}(t)$. Since for the stage $(J + P)$, both its input and the injection signal could be regarded as being time delayed by Pk/f_{inj} from stage J , the response at stage $(J + P)$ is expected to be the same as stage J , only being time delayed by Pk/f_{inj} .

Assuming that the injection signal amplitude is small compared to V_{GS} , the bias current $I_b(t)$ is expressed as

$$I_b(t) = I_B + g_{m_{inj}} V_{INJ} \sin(\omega_{inj} t + \phi) \quad (6)$$

where V_{INJ} is the amplitude of the injection signal.

Similar to the above discussion for the free running ILFD, we study the output response to $I_b(t)U(t)$ whose initial voltage level is V_{DD} . Again, we model this response as a current source discharging C_{out} in parallel with R_{out} . After solving the differential equation associated with the RC load, $V_{out}(t)$ can be approximated as (7). If the ILFD is locked to the injection signal, t_{d-osc} has to be equal to k/f_{inj} . According to (7), $V_{out}(t_{d-osc})$ is expressed as (8). It is assumed that t_{d-osc} is defined as the time required to go from V_{DD} to $V_{DD} - |V_{TP}|$, so that $V_{out}(k/f_{inj}) = V_{DD} - |V_{TP}|$. However, for a fixed injection signal amplitude V_{INJ} , using the inequality given in (9), $V_{out}(k/f_{inj})$ is bounded the limits obtained in (10). Thus, the following inequality (11) is derived, setting the range of the injection frequency for a certain circuit implementation and given injection signal amplitude.

It is difficult to get an analytical solution for f_{osc} from (11). However, some insights could still be derived. If $V_{INJ} = 0$, i.e., there is no signal injected, as expected, (11) has only one solution, which is $f_{osc} = f_{osc-fr}$. In other words, this indicates that the free running oscillation frequency f_{osc-fr} falls into the locking range. With the increase of V_{INJ} , the range of f_{osc} that meets (11) is extended. (11) also predicts the existence of multiple division ratios, shown as $2kN$, as k appears in (11). However, with larger k , the conditions for f_{osc} to meet the inequality become tight, leading to the decrease of the locking range

$$\begin{aligned} V_{out}(t) &= V_{DD} - I_B R_{out} (1 - e^{-t/R_{out}C_{out}}) \\ &\quad - g_{m_{inj}} V_{INJ} \cos \phi \frac{R_{out}}{1 + (R_{out}C_{out}\omega_{inj})^2} (\sin \omega_{inj} t) \\ &\quad - R_{out} C_{out} \omega_{inj} \cos \omega_{inj} t + R_{out} C_{out} \omega_{inj} e^{-t/R_{out}C_{out}} \\ &\quad - g_{m_{inj}} V_{INJ} \sin \phi \frac{R_{out}}{1 + (R_{out}C_{out}\omega_{inj})^2} (\cos \omega_{inj} t) \\ &\quad + R_{out} C_{out} \omega_{inj} \sin \omega_{inj} t - e^{-t/R_{out}C_{out}} U(t) \end{aligned} \quad (7)$$

$$\begin{aligned} V_{out}(k/f_{inj}) &= V_{DD} - I_B R_{out} (1 - e^{-2k\pi/R_{out}C_{out}\omega_{inj}}) \\ &\quad \times \left[1 + \frac{g_{m_{inj}} V_{INJ} (-R_{out}C_{out}\omega_{inj} \cos \phi + \sin \phi)}{I_B (1 + (R_{out}C_{out}\omega_{inj})^2)} \right] \end{aligned} \quad (8)$$

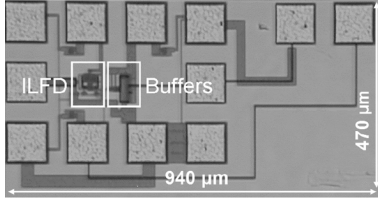


Fig. 5. Chip micro photograph.

$$| -R_{out}C_{out}\omega_{inj} \cos \phi + \sin \phi | \leq \sqrt{1 + (R_{out}C_{out}\omega_{inj})^2} \quad (9)$$

$$\begin{aligned} & V_{DD} - I_B R_{out} \left(1 - e^{-2k\pi/R_{out}C_{out}\omega_{inj}} \right) \\ & \times \left(1 + \frac{g_{m_{inj}} V_{INJ}}{I_B} \frac{1}{\sqrt{1 + (R_{out}C_{out}\omega_{inj})^2}} \right) \\ & \leq V_{out}(k/f_{inj}) \leq \\ & V_{DD} - I_B R_{out} \left(1 - e^{-2k\pi/R_{out}C_{out}\omega_{inj}} \right) \\ & \times \left(1 - \frac{g_{m_{inj}} V_{INJ}}{I_B} \frac{1}{\sqrt{1 + (R_{out}C_{out}\omega_{inj})^2}} \right) \end{aligned} \quad (10)$$

$$\begin{aligned} & \left| 1 - \frac{|V_{TP}|}{\left(1 - (1 - |V_{TP}|/I_B R_{out}) \frac{f_{osc_fr}}{f_{osc}} \right) I_B R_{out}} \right| \\ & \leq \frac{g_{m_{inj}} V_{INJ}}{I_B} \frac{1}{\sqrt{1 + \left(\frac{2k\pi}{\ln(1 - |V_{TP}|/I_B R_{out})} \frac{f_{osc_fr}}{f_{osc}} \right)^2}} \end{aligned} \quad (11)$$

IV. CIRCUIT IMPLEMENTATION AND MEASUREMENT RESULTS

To verify circuit's performance, a three-stage ILFD was implemented in a standard 0.18- μm CMOS technology. A differential three-stage buffer chain is connected from one of the three stages to pads for testing purpose. To balance the load for all the stages, buffers identical to the first buffer in the buffer chain are also connected to the other two stages.

Fig. 5 shows the micro photograph of the frequency divider with output buffers. The chip area is $940 \times 470 \mu\text{m}^2$ including the contact pads. The core of the frequency divider and the buffer chain occupy $77 \times 66 \mu\text{m}^2$ and $88 \times 71 \mu\text{m}^2$, respectively. The measurement was performed on a standard FR4 PC board. The injection signal is generated from a HP 8673C synthesized signal generator while the phase noise is measured through a R&S FSEB 30 spectrum analyzer. Both the injection signal and the dc bias voltage are applied to the gate of the tail current source transistor through a bias tee. Because of the limited bandwidth of the bias tee (4.2 GHz), the injection signal at high frequency is attenuated. For instance, the measured attenuation at 6 GHz is 2.2 dB. The attenuation measurement are limited by the upper range of our spectrum analyzer (7 GHz). Fig. 6 shows the phase noise of the locked output signal with the division ratio of 12 when the injection frequency is 7.2 GHz. As a reference, the phase noises of the signal generator at 7 GHz (the highest frequency that could be measured by the spectrum analyzer) are -95 dBc/Hz and -120 dBc/Hz , at 10 kHz and 500 kHz offset respectively. We could not obtain the phase noise plot for the free running ILFD, because without the input signal,

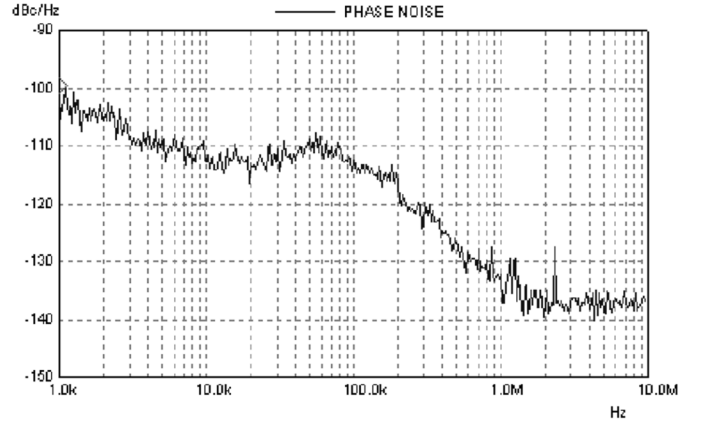


Fig. 6. Measured output phase noise of the ILFD for the division ratio of 12 with injection frequency of 7.2 GHz.

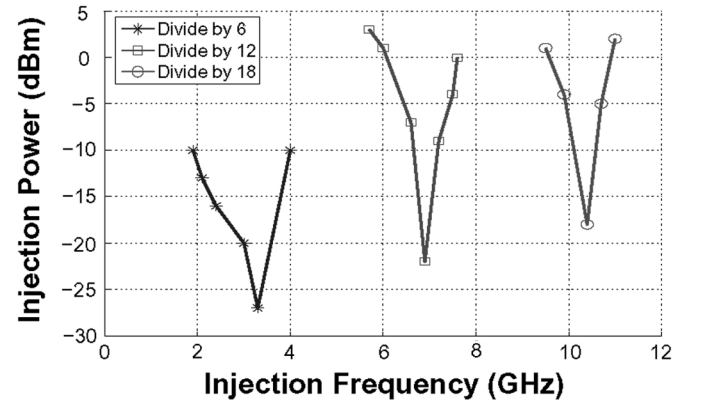


Fig. 7. Measured input sensitivity.

the center frequency is not stable since any voltage variation present at the bias input changes the bias current. As indicated in (4) and (5), the free running oscillation frequency is fluctuated by the noise added to I_B . It is, however, another way to show that the ILFD was locked to the external signal.

The measured average free running oscillation frequency is 562 MHz, which is 20% below the simulated value. This result shows that the parasitic capacitance was underestimated. The measured input sensitivity of the ILFD is shown in Fig. 7. It shows that higher input power is needed for higher division ratio. There are two reasons. Firstly, the frequency dependent attenuation of the bias tee is not accounted for. Secondly, the parasitic capacitance at the common source node further attenuates the injection signal, especially at high frequencies. The unaccounted bias tee loss prevents us from collecting realistic input power data. Other than this, the maximum injection frequency is 11.2 GHz with the division ratio of 18. As the measured power consumption is 7.2 mW, using the figure of merit (FoM) defined in [8], which is the maximum injection frequency per unit power consumption, the FoM for this ILFD is 1.5 GHz/mW. This figure is not rated excellent among the frequency dividers listed in [8]. However, the larger division ratio achieved in this ILFD helps to reduce the power consumption of the following frequency division stages since they operate at lower frequencies.

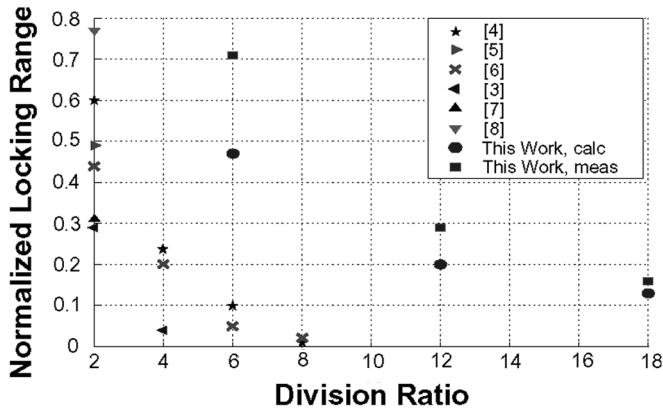


Fig. 8. Comparison of normalized locking range versus division ratio.

TABLE I
PERFORMANCE SUMMARY

Technology	0.18 μm CMOS
Supply Voltage	1.8 V
Power Dissipation	7.2 mW
Active Area	$0.17 \times 0.14 \text{ mm}^2$
Divide-by-6 Locking Range	1.9 – 4.0 GHz
Divide-by-12 Locking Range	5.7 – 7.6 GHz
Divide-by-18 Locking Range	9.5 – 11.2 GHz

Fig. 7 shows that for the division ratios of 6, 12, and 18, the locking ranges are 2.1, 1.9, and 1.7 GHz, respectively. To compare the measured locking range results with the numeric calculation results and the published ones, we normalized all locking range data to their center frequencies. Fig. 8 shows the normalized locking range of this work and other published data against division ratio [3]–[8]. The proposed architecture achieves the best normalized locking range so far. Of all the previously published results, only one with division ratio of 2 [8] has larger normalized locking range than the proposed topology with division ratio of 6. However, that solution only outputs pseudo differential signals. Division ratios larger than 8 with acceptable locking ranges are not reported in any of the previous publications. The graph shows a general downward trend, with the normalized locking range decreasing as the division ratio increases. Compared with the measurement results, the theoretical results show large discrepancies at the lowest division ratio. This is because we assume weak injection in our model, while in the measurement we applied relatively large injection signal power. The discrepancy becomes less as the division ratio goes

higher. Again, this is because the attenuation of the bias tee and the under-estimated parasitic capacitance reduce the measured locking range. The performance of the measured ILFD is summarized in Table I.

V. CONCLUSION

A CMOS three stage ring ILFD has been demonstrated for the proposed multiple highly nonlinear injection stage and large division ratio ILFD architecture. Measurement results show the ILFD fabricated in a standard $0.18\text{-}\mu\text{m}$ CMOS process achieves multiple large division ratios of 6, 12, and 18 with locking range greater than 1.7 GHz, for a power consumption of 7.2 mW from a 1.8 V power supply.

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