

Steady-State Analysis of Phase-Locked Loops Using Binary Phase Detector

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Abstract—Phase-locked loops (PLLs) using binary phase detectors (BPDs) are modeled and analyzed in this paper. Steady-state behavior for PLLs based on BPDs (BPLs) using first- and second-order loop filters is characterized using transient waveform equations. It is shown that BPLL has a range of oscillation modes in steady state when there is no input jitter. The BPLL is most likely to operate at the most stable oscillation mode (MSOM) under the disturbance of random input jitter. The MSOM is determined by evaluating the relative stability of all the modes. The expected value of the output jitter amplitude is derived and its dependence on the loop parameters is analyzed.

Index Terms—Bang-bang phase detector (BPD), binary phase-detector, clock-and-data recovery (CDR), phase-locked loop (PLL).

I. INTRODUCTION

PHASE-LOCKED loops (PLLs) using binary phase detectors (BPDs) are receiving more attention with the ever-increasing demand for higher operational frequency. BPDs are also called bang-bang phase detectors (PDs). BPDs output a high or low level depending on the sign of the input phase difference. The advantage of BPDs over linear phase detectors is that BPD can operate at higher speed without suffering from dead-zone problems or component mismatches [1]. PLLs based on BPDs (BPLLs), have found many applications in systems that require ultra-high-speed reference signals with frequencies comparable to the voltage-controlled oscillator (VCO) frequency. Examples include multi-gigahertz clock multipliers [2], optical receivers (STM, SONET) [1], [3], and high-speed serial data links (SATA, PCI Express) [4].

BPLLs are a nonlinear system due to the nonlinear phase-to-voltage transfer curve of the BPD. It is a hybrid structure between a continuous-time and a discrete-time system because the filter and VCO behave as continuous-time modules while the BPD works via discrete-time sampling. Many efforts have been spent on the nonlinear loop dynamics of BPLLs [5]–[9]. [5] analyzed the lock-in behavior of BPLLs. [6]–[8] mainly focus on the characterization of jitter transfer and tolerance properties of BPLLs in response to large sinusoidal input jitter without detailed analysis of the steady-state behavior of the loop itself. The steady-state solutions of BPLL with zero and first-order digital filters are investigated in [9] using a discrete-time iterative

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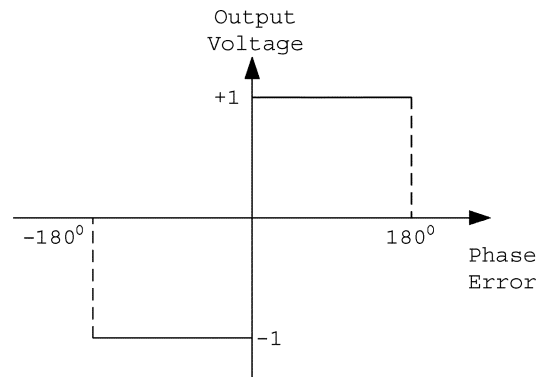


Fig. 1. Transfer characteristic of an ideal BPD.

method. It reveals the existence of multiple orbits but fails to indicate which orbit the loop will take in actual operation. Also, BPLLs with analog or second-order filters were not discussed.

The nonlinear loop dynamics of BPLLs are modeled and analyzed in detail in this work using both discrete-time and continuous-time analysis. The steady-state solutions of BPLL with first- and second-order analog loop filters are derived in Section II. The existence of multiple oscillation modes is revealed and the most stable mode is found by evaluating the tolerance to the jitter disturbance. Section III draws conclusions from this work.

II. STEADY-STATE ANALYSIS OF BPLL

BPLLs are PLLs which detect the phase difference between the reference signal and feedback signal using a BPD. The reference signal can be periodic or a random bit sequence. Particularly, when the incoming signal is random data, the BPLL becomes a binary clock-and-data recovery circuit (BCDR). CDR is a special type of PLL which recovers clock and data signal from a random bit sequence. The transfer characteristic of an ideal BPD is shown in Fig. 1. The BPD outputs +1 and -1 for positive and negative phase error, respectively. Actual implementations of BPDs are usually affected by metastability and jitter. These effects are discussed in [8] and not considered here for simplicity. The phase-domain block diagram of a BPLL is shown in Fig. 2. The symbol I represents the charge pump (CP) output current and K represents the VCO gain. The loop delay cell models the lumped delay (t_d) from all the building blocks. It is usually caused by buffers and logic gates used throughout the loop. The frequency divider module is optional depending on the actual implementation. For simplicity, it will be ignored in the following analysis since it is just a gain factor in the phase

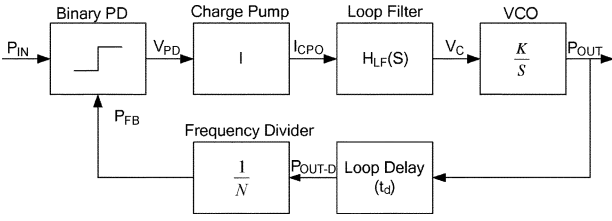


Fig. 2. Phase-domain model of PLL based on BPD.

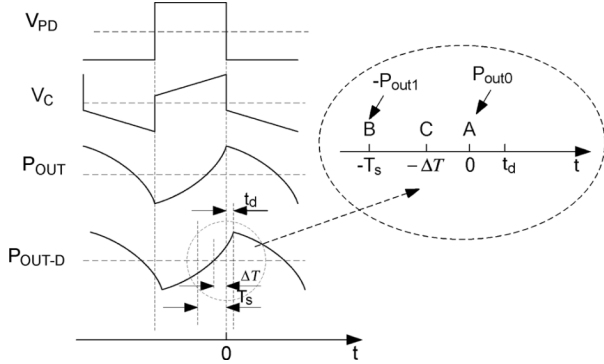


Fig. 3. Steady-state waveforms of BPLL with first-order filter.

domain. The phase-domain model in Fig. 2 was implemented as a behavioral prototype using Simulink modules in Matlab to verify the correctness of the derived expressions. The steady-state behaviors of a BPLL with first-order and second-order filters in the absence of input jitter were simulated and analyzed.

Since the BPD samples the phase error at the edge of the output signal, the BPLL is actually a sampling system. Although the sampling period varies with the change of the phase of the VCO, the output phase has very small variation when the BPLL is fully locked. Since this work focuses on steady-state analysis only, the sampling period is assumed to be constant (denoted as T_S) to simplify the analysis. The simulation time step is set as $T_S/20$ for reasonable accuracy.

A. BPLL With First-Order Loop Filter

The first-order loop filter is the series combination of a resistor R and a capacitor C (refer to Fig. 5, shown later, without C_2) to convert the CP current into voltage. It is widely used in practical implementations of BPLL and BCDR [1]–[3]. In some digital implementations [2], the first-order loop filter is split into a proportional branch and an integral branch. The steady-state waveforms of the BPLL prototype with a first-order filter are drawn illustratively for better understanding in Fig. 3. It can be reasonably assumed that all the steady-state waveforms are symmetric around zero and have the same period of T_P in steady state. Note that T_P has nothing to do with the time-domain oscillation period of the VCO. Since the BPD output is just the sign of phase error, it must be a square wave of 50% duty cycle with period of T_P in the absence of input jitter. Thus, the waveform of VCO control voltage (V_C) is obtained as

$$V_C(t) = \begin{cases} \frac{It}{C} + IR + \frac{IT_P}{4C}, & -\frac{T_P}{2} < t < 0 \\ -\frac{It}{C} - IR + \frac{IT_P}{4C}, & 0 < t < \frac{T_P}{2}. \end{cases} \quad (1)$$

The output phase is derived as the integration of $KV_C(t)$

$$P_{OUT} = \begin{cases} K \left(\frac{It^2}{2C} + IRt + \frac{T_P It}{4C} + \frac{IRT_P}{4} \right), & -\frac{T_P}{2} < t < 0 \\ K \left(-\frac{It^2}{2C} - IRt + \frac{T_P It}{4C} + \frac{IRT_P}{4} \right), & 0 < t < \frac{T_P}{2}. \end{cases} \quad (2)$$

The peak of the output phase occurs at $t = 0$, which is obtained from (2) as

$$A_{OUT} = P_{OUT}(0) = \frac{IKRT_P}{4}. \quad (3)$$

Please note that the initial conditions for the output phase and control voltage are derived based on the assumption of symmetry around zero.

It can be seen from (3) that the output phase amplitude is proportional to R and T_P . However, it does not depend on the capacitor. As shown in Fig. 3, the peaks of P_{OUT} are aligned with the transition edges of V_{PD} . The zero-crossing time of P_{OUT-D} (point C) must sit between point A (where the BPD switches) and point B (the sampling instant immediately preceding point A). Otherwise, the BPD would have switched at point B instead of point A. Denoting the values of P_{OUT-D} at point A and B as $|P_{OUT0}|$ and $-|P_{OUT1}|$, these conditions can be expressed as

$$\begin{cases} |P_{OUT0}| = P_{OUT-D}(0) = P_{OUT}(-t_d) > 0 \\ -|P_{OUT1}| = P_{OUT-D}(-T_S) = P_{OUT}(-t_d - T_S) < 0. \end{cases} \quad (4)$$

The range of the oscillation period T_P can be solved by substituting (2) into (4) and the result is obtained as

$$\begin{aligned} T_{MIN} &= \frac{2t_d(2RC - t_d)}{RC - t_d} < T_P \\ &< \frac{2(T_S + t_d)(2RC - T_S - t_d)}{RC - T_S - t_d} \\ &= T_{MAX}. \end{aligned} \quad (5)$$

The above range is derived based on the condition $RC > T_S + t_d$ which is satisfied in most practical designs and ensures the stability of the BPLL. Since the BPD output has 50% duty cycle and each half cycle must be a multiple of T_S , the complete cycle T_P must be an even multiple of T_S as

$$T_P = 2nT_S, \quad n = 1, 2, 3, \dots \quad (6)$$

Combining (5) and (6), it can be concluded that T_P must be an even multiple of T_S staying within the upper limit T_{MAX} and the lower limit T_{MIN} . An interesting conclusion indicated by (5) is that the BPLL is able to oscillate within a range of oscillation periods (modes) in steady state. This fact is similar to the existence of multiple orbits for digital PLLs indicated in [9]. The actual oscillation mode depends on the initial voltage on the loop filter capacitor and the initial output phase of the VCO. The initial voltage on the capacitor required to reach a particular oscillation period can be derived from (1) as follows:

$$V_{C0} = V_C(0) = IR + \frac{IT_P}{4C}. \quad (7)$$

The initial phase of the VCO is simply the value of $P_{\text{OUT}}(0)$ given by (3). The initial voltage and phase can be applied so that the BPLL enters the corresponding oscillation mode immediately without additional settling in Matlab simulations.

When the loop delay t_d is zero, T_{MIN} is zero and the actual lower limit for the possible oscillation periods becomes $2T_S$. When the loop delay is much larger than one sampling period, i.e., $t_d \gg T_S$, T_{MIN} is very close to T_{MAX} and the BPLL oscillates within a small frequency band in steady state. In this case, the BPLL can be assumed to have only one mode equal to $(T_{\text{MAX}} + T_{\text{MIN}})/2$. It can be seen from (5) that the BPLL tends to oscillate at longer periods with the increase of the loop delay, which is consistent with intuition since longer latency decreases the response time of the loop.

When $RC \gg T_S$, the voltage variations on the capacitor can be ignored in steady state. Under this condition, the behavior of the BPLL closely resembles the behavior of BPLL with zeroth-order loop filter, i.e., a simple resistor; the values for T_{MIN} and T_{MAX} can be approximated as

$$4t_d \approx T_{\text{MIN}} < T_p < T_{\text{MAX}} \approx 4(T_S + t_d). \quad (8)$$

It can be seen that the BPLL has only two oscillation periods within the given range for T_P . When $t_d \gg T_S$, these two periods are proportional to the loop delay. In the special case when $t_d = 0$ and $C = \infty$, it results in $T_{\text{MIN}} = 0$ and $T_{\text{MAX}} = 4T_S$; thus, the BPLL has only one oscillation mode with $T_P = 2T_S$.

Although the BPLL is able to have a range of sustainable oscillation modes in the noise-free case, the steady states associated with each oscillation mode may be broken if the input jitter is large enough to change the decision of the BPD. When the input jitter stays smaller than both $|P_{\text{OUT}0}|$ and $|P_{\text{OUT}1}|$ as defined in (4) (refer to Fig. 3), the BPD output is exactly the same as the noise-free case; the BPLL sustains its original oscillation mode without being disturbed. On the other hand, if the maximum input jitter is larger than either $|P_{\text{OUT}0}|$ or $|P_{\text{OUT}1}|$, the BPD will make different decisions from the zero-input case. The original steady state will be broken and the loop may settle to a different oscillation mode. Therefore, we can define the following index to measure the relative stability of each oscillation mode

$$D_{\text{stable}} = \min(|P_{\text{OUT}0}|, |P_{\text{OUT}1}|). \quad (9)$$

The most stable oscillation mode (MSOM) can be determined by finding the maximum value of D_{stable} . When Gaussian input jitter (virtually unbounded) is applied, the BPLL is expected to settle to the MSOM at the greatest probability among all the modes. The values of $|P_{\text{OUT}0}|$ and $|P_{\text{OUT}1}|$ across all the oscillation modes under a test case ($RC/T_S = 4$ and $t_d = T_S$) is shown in Fig. 4. $|P_{\text{OUT}0}|$ increases and $|P_{\text{OUT}1}|$ decreases monotonically with the increase of T_P . It is easy to see that the maximum value of D_{stable} occurs when $|P_{\text{OUT}0}| = |P_{\text{OUT}1}|$. Thus, based on the definition of $|P_{\text{OUT}0}|$ and $|P_{\text{OUT}1}|$ in (4), the following equation must be satisfied at the MSOM

$$P_{\text{OUT}}(-t_d - T_S) + P_{\text{OUT}}(-t_d) = 0. \quad (10)$$

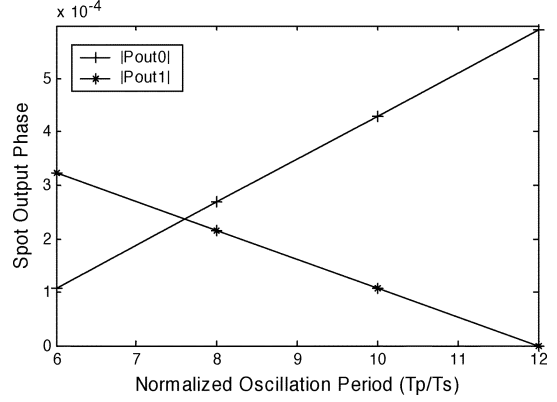


Fig. 4. $|P_{\text{OUT}0}|$ and $|P_{\text{OUT}1}|$ across all the modes for BPLL with first-order filter.

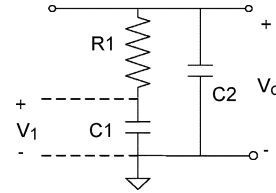


Fig. 5. Second-order loop filter.

The period of the MSOM is derived by solving (10), yielding

$$T_{P\text{-stable}} = \frac{(T_s + 2t_d)(4RC - T_s - 2t_d) - T_S^2}{2RC - T_s - 2t_d}. \quad (11)$$

This result was verified by simulations. When Gaussian input jitter is applied, the oscillation period of the BPLL does settle to values around $T_{P\text{-stable}}$ as predicted. The BPLL may operate at a few modes around the MSOM since Gaussian input jitter is unbounded and the MSOM may be broken as well. Hence, in the presence of jitter disturbance, the expected value of the output jitter amplitude is equal to the output jitter amplitude at the MSOM and it is obtained from (3) as

$$\overline{A_{\text{OUT}}} = P_{\text{OUT}}(0)|_{T_P=T_{P\text{-stable}}} = \frac{IKRT_{P\text{-stable}}}{4}. \quad (12)$$

Notice that the input jitter disturbance here is considered weak and its contribution is not included in the value of A_{OUT} . In actual operation, the BPLL moves back and forth around the MSOM due to the jitter disturbance. The variance from the MSOM depends on the strength of the input jitter disturbance. It can be seen from (11) that $T_{P\text{-stable}}$ increases with the decrease of RC and the increase of t_d ; so does the expected output jitter amplitude. Therefore, the capacitor value should be maximized to minimize the output jitter within limits imposed by the locking time. On the other hand, the loop delay should also be minimized to reduce the output jitter.

B. BPLL With Second-Order Filter

The schematic of a second-order filter is shown in Fig. 5. It adds C_2 , a capacitor usually much smaller than C_1 , in addition to the first-order filter. Similarly, the steady-state waveforms of BPLLs with second-order filters are assumed to be periodic and symmetric around zero. Following the same approach used in

the first-order filter, the expression for VCO control voltage is derived as

$$V_C(t) = \begin{cases} V_0 \left(1 - \frac{2e^{-t/\tau}}{1+e^{-T_P/2\tau}} \right) + \frac{I(t-T_P/4)}{C_1+C_2}, & 0 < t < T_P/2 \\ V_0 \left(-1 + \frac{2e^{-(t-T_P/2)/\tau}}{1+e^{-T_P/2\tau}} \right) - \frac{I(t-3T_P/4)}{C_1+C_2}, & T_P/2 < t < T_P \end{cases} \quad (13)$$

where $V_0 = \frac{IRC_1^2}{(C_1+C_2)^2}$; $\tau = R(C_1||C_2)$.

The initial voltages on C_1 and C_2 when $t = 0$ are also obtained as (14), shown at the bottom of the page. The output phase can be derived as the integration of KV_C from (13) resulting in

$$P_{OUT}(t) = K \left[V_0 \left(t - \frac{T_P}{4} - \tau \right) + \frac{2V_0\tau e^{-t/\tau}}{1+e^{-T_P/2\tau}} + \frac{It(2t-T_P)}{4(C_1+C_2)} \right] \quad \text{when } 0 < t < \frac{T_P}{2}$$

$$P_{OUT}(t) = -K \left[V_0 \left(t - \frac{3T_P}{4} - \tau \right) + \frac{2V_0\tau e^{(T_P-t)/\tau}}{1+e^{-T_P/2\tau}} + \frac{It(t-T_P)}{2(C_1+C_2)} \right] \quad \text{when } \frac{T_P}{2} < t < T_P. \quad (15)$$

The initial output phase of the VCO is then derived as

$$P_{OUT}(0) = KV_0 \left(\tau \tanh \left(\frac{T_P}{4\tau} \right) - \frac{T_P}{4} \right). \quad (16)$$

The time when P_{OUT} reaches the minimum value can be derived by finding the zero-derivative point of (15). The result is obtained as

$$t_{\min} = \text{LambertW} \left(\frac{C_1 e^{\frac{C_1}{C_2}}}{C_2 \cosh \left(\frac{T_P}{4\tau} \right)} \right) \tau - \frac{V_0(C_1+C_2)}{I} + \frac{T_P}{4}. \quad (17)$$

LambertW(z) [10] is a special function whose value is the solution of the following:

$$z = xe^x. \quad (18)$$

To get more insight on the characteristic of t_{\min} , we assume $C_1 \gg C_2$ and $\tau > T_P$; these are typical conditions for second-

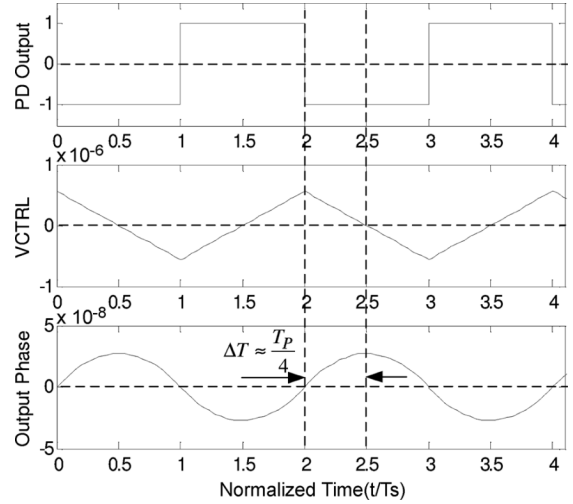


Fig. 6. Steady-state waveforms of BPLL with second-order filter ($K_{VCO} = 1.9$ GHz/V, $R = 56 \Omega$, $C_1 = 35$ nF, $C_2 = 3.5$ nF, $T_P = T_d = 0.2$ ns, $T_S = 0.1$ ns).

order filters used in practical implementations of BPLL. Under these assumptions, (17) can be further simplified as

$$t_{\min} \approx \text{LambertW} \left(\frac{C_1}{C_2} e^{\frac{C_1}{C_2}} \right) \tau - \frac{V_0(C_1+C_2)}{I} + \frac{T_P}{4} = \frac{T_P}{4}. \quad (19)$$

Substituting (19) into (15), the output phase amplitude is obtained as

$$A_{OUT} = |P_{OUT}(t_{\min})| \approx \frac{KIT_P^2}{32(C_1+C_2)} + KV_0\tau \left(1 - \frac{1}{\cosh \left(\frac{T_P}{4\tau} \right)} \right). \quad (20)$$

Under the typical conditions $\tau > T_P$ and $C_1 \gg C_2$, A_{OUT} can be further simplified by way of second-order Taylor series expansion

$$A_{OUT} \approx \frac{KIT_P^2}{32C_2}. \quad (21)$$

Equation (21) indicates that the output phase amplitude is approximately proportional to the square of the oscillation period while inversely proportional to the smaller capacitor in the filter. It is still proportional to VCO gain and CP current as in the case of first-order filters. However, it no longer depends on the filter resistor. The prototype BPLL was simulated with second-order filter and the steady-state waveforms are shown in Fig. 6. It verifies that the peaks and valleys of the output phase are actually

$$V_{10} = \frac{-I \left[e^{-\frac{T_P}{2\tau}} (T_P + 4R(C_1||C_2)) + T_P - 4R(C_1||C_2) \right]}{4(C_1+C_2) \left(1 + e^{-\frac{T_P}{2\tau}} \right)}$$

$$V_{C0} = \frac{-I \left[e^{-\frac{T_P}{2\tau}} \left(T_P - 4R(C_1||C_2) \frac{C_1}{C_2} \right) + T_P + 4R(C_1||C_2) \frac{C_1}{C_2} \right]}{4(C_1+C_2) \left(1 + e^{-\frac{T_P}{2\tau}} \right)} \quad (14)$$

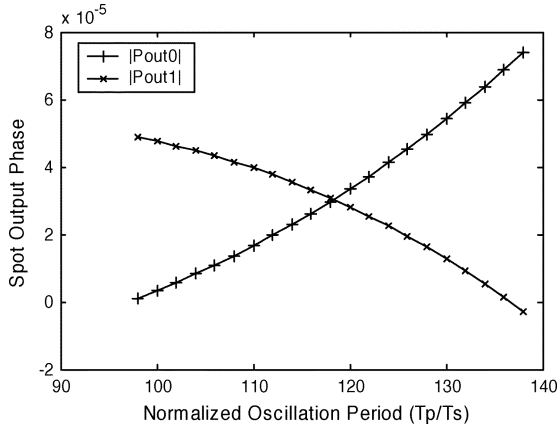


Fig. 7. $|P_{OUT0}|$ and $|P_{OUT1}|$ versus oscillation periods for BPLL with second-order filter.

located around $T_P/4$ from the zero-crossing points as indicated by (19).

Multiple oscillation modes also exist in the steady state of BPLLs with second-order filters. Similar to the analysis of BPLLs with first-order filters, the zero-crossing point of the output phase must sit between the switching instant of the BPD and the immediately preceding sampling instant. Thus, the same constraint expressed by (4) applies. Substituting (15) into (4) and using third-order Taylor series approximation under the typical condition $\tau \gg T_S + t_d$ and $T_P \gg T_S$, the range of T_P is obtained as

$$\sqrt{48RC_2 t_d} \approx T_{\text{MIN}} < T_P < T_{\text{MAX}} \approx \sqrt{48RC_2(T_S + t_d)}. \quad (22)$$

Thus, the BPLL can oscillate at any even multiples of T_S between T_{MAX} and T_{MIN} . All the oscillation modes can be produced in simulation by applying the initial conditions given by (14) and (16). When $t_d \gg T_S$, T_{MIN} is close to T_{MAX} and the BPLL can only oscillate within a narrow frequency band.

When the BPLL has Gaussian input jitter, the MSOM can be determined using the same index D_{stable} defined in (10) for the analysis of BPLL with first-order loop filter. The values for $|P_{OUT0}|$ and $|P_{OUT1}|$ (defined in (9)) across all the possible modes under a test case ($C_1/C_2 = 100$, $T_S = t_d$, $\tau/T_S \approx 200$) are plotted in Fig. 7. $|P_{OUT0}|$ increases monotonically while $|P_{OUT1}|$ decreases monotonically with the increase of T_P . Notice that the maximum value of D_{stable} occurs when $|P_{OUT0}| = |P_{OUT1}|$. Thus, the oscillation period at the MSOM ($T_{P\text{-stable}}$) can be determined by solving the following:

$$P_{\text{OUT}}(-t_d - T_S) = -P_{\text{OUT}}(-t_d). \quad (23)$$

If we assume that the output jitter changes linearly with time in one sampling period (typically true since BPLLs are usually used in multi-gigahertz applications with $T_S \ll 0.1$ ns), (23) can be approximated by the following:

$$P_{\text{OUT}}\left(-t_d - \frac{T_S}{2}\right) = 0. \quad (24)$$

Solving (24) yields the solution for $T_{P\text{-stable}}$

$$T_{P\text{-stable}} \approx \sqrt{48RC_2 \left(\frac{T_S}{2} + t_d\right)}. \quad (25)$$

The expected value of the output jitter amplitude is equal to the output jitter amplitude at the MSOM. It is derived by substituting (25) into (21)

$$\overline{A_{\text{OUT}}} = \frac{KIT_{P\text{-stable}}^2}{32C_2} \approx \frac{3}{4}KIR(T_S + 2t_d). \quad (26)$$

Equation (26) shows that under the conditions $\tau \gg T_S + t_d$ and $T_P \gg T_S$, the expected output jitter amplitude is proportional $T_S + 2t_d$ but independent of either C_1 or C_2 .

III. CONCLUSION

The steady-state behavior of BPLLs was investigated by combining discrete-time and continuous-time analysis. Accurate equations are derived to describe the steady-state solutions. The analysis shows that the BPLLs can have a range of oscillation modes in steady state. Under the disturbance of random jitter, the BPLL is expected to settle to the MSOM, which can be determined by evaluating the relative stability of all the modes. The expected value of the output jitter amplitude is derived and its dependence on the loop parameters is analyzed. The results in this work help designers to estimate and optimize the jitter performance of BPLLs in system-level design.

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