

# A 92 MHz, 13 Bit IF Digitizer Using Optimized SC Integrators in 0.35 $\mu\text{m}$ CMOS Technology

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**Abstract**—A feedforward compensation scheme with no Miller capacitors is proposed to overcome the bandwidth limitations of traditional Miller compensation schemes. The technique has been used in the design of an operational transconductance amplifier (OTA) with a DC gain of 80 dB, GBW of 1.4 GHz, phase margin of  $62^\circ$  and 2 ns settling time for 2 pF load capacitor in a standard 0.35  $\mu\text{m}$  CMOS technology. The OTA's current consumption is 4.6 mA. The OTA is used in the design of a fourth order switched capacitor bandpass  $\Sigma\Delta$  modulator with a clock frequency of 92 MHz. It achieves a peak SNR of 80 dB and 54 dB for 270 kHz (GSM) and 3.84 MHz (CDMA) bandwidths, respectively and consumes 19 mA of current from a  $\pm 1.25$  V supply.

**Index Terms**—feedforward compensation, pole zero doublet, bandpass sigma-delta modulator, analog-to-digital converter

## I. INTRODUCTION

Bandpass sigma-delta ( $\Sigma\Delta$ ) modulators are widely used for direct digitization of narrowband signals around an intermediate frequency in a radio receiver. The main emphasis of research in bandpass  $\Sigma\Delta$  ADC's is to increase the center frequency with a negligible increase in power consumption. The maximum achievable center frequency is directly related to the clock frequency, which is typically limited by the speed of the switched capacitor integrator. Various architectural level techniques such as two-path architecture [1], double sampling resonator [2], double sampling with pseudo two paths [3] and double delay resonator [4] have been proposed to improve the effective clock frequency of bandpass  $\Sigma\Delta$  modulators. These architectural techniques relax the requirements of the amplifier performance. In this work, we examine the limitations of switched capacitor circuits and use a compensation technique to improve the speed of the amplifier. The amplifier is used in the design of a high speed bandpass  $\Sigma\Delta$  analog to digital converter.

## II. DESIGN CONSIDERATIONS

A switched capacitor (SC) integrator in feedback operation during the integrating clock phase is shown in Fig. 1. The closed loop transfer function during the integrating phase is given by

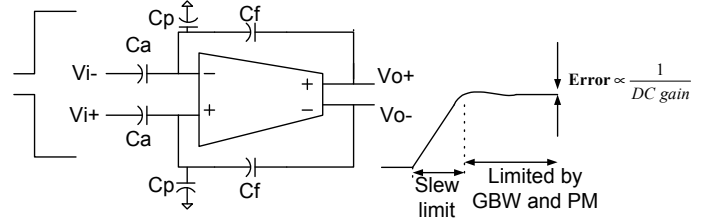


Fig. 1. Closed loop operation of a switched capacitor integrator

$$\frac{V_o}{V_i} \cong \frac{\alpha A_{v0} \omega_p}{s + (1 + \beta A_{v0}) \omega_p} \quad (1)$$

$$\alpha = \frac{C_a}{C_a + C_f + C_p} \quad \beta = \frac{C_f}{C_a + C_f + C_p}$$

where  $\alpha$  is the feedforward factor,  $\beta$  is the feedback factor,  $A_{v0}$  is the open loop DC gain of the amplifier,  $\omega_p$  is the amplifier's dominant pole,  $C_p$  is the sum of all parasitic capacitances at the input node of amplifier and  $C_a, C_f$  are the input and feedback capacitors.

Assuming an amplifier with an equivalent single pole response, as shown in (1), and following a similar procedure as [8], the output step response of the SC integrator after the slewing phase is given by

$$V_{out}(t) = - \left( \frac{\frac{C_a}{C_f}}{1 + \frac{1}{\beta A_{v0}}} \right) \left( 1 - e^{-\beta \omega_{GBW} t} \right) V_{in} + V_o(t_0) \quad (2)$$

where  $\omega_{GBW}$  ( $=A_{v0}\omega_p$ ) is the gain-bandwidth product of the amplifier and  $V_o(t_0)$  is the initial condition at the output node. The amplifier's settling consists of two phases: slew rate and linear settling dictated by the  $\omega_{GBW}$  and phase margin of the amplifier [8]. The error in the final settling is inversely proportional to amplifier's DC gain and speed is proportional to  $\omega_{GBW}$ . For a good settling performance, the amplifier must have a high gain along with high  $\omega_{GBW}$  and good phase margin. The exponential term in (2),  $\beta\omega_{GBW}$ , should be large such that the output settles properly within one-half of the clock period ( $T_{clock}$ ). For a settling error below 0.25 % during the integrating clock phase,  $\beta\omega_{GBW}T_{clock}/2$  must be greater than 6. For a closed loop switched capacitor feedback amplifier with a feedback factor of  $\beta$ , the relationship between clock frequency  $f_{clock}$  ( $1/T_{clock}$ ), the integrating time  $T_{integration}$

( $\delta T_{\text{clock}}/2 = \delta/2f_{\text{clock}}$ ) and the amplifier's  $\omega_{\text{GBW}}$  ( $=2\pi f_{\text{GBW}}$ ) is

$$f_{\text{GBW}} > \frac{n}{2\pi\beta T_{\text{integration}}} = \frac{nf_{\text{clock}}}{\delta\pi\beta} \quad (3)$$

where  $n$  is defined according to the required accuracy;  $n=6$  for 0.25 % accuracy and 8 for an accuracy of 0.033 %.  $\delta T_{\text{clock}}/2$  is the effective time for linear settling available after non-overlapped clock generation.  $\delta$  is usually in the range of 0.5-0.8. For the  $\Sigma\Delta$  modulator described in section IV, the operating conditions of the integrators during the integrating phase are given in Table I. For the smallest  $\beta$ ,  $\delta=1$  and a clock frequency of 100 MHz, the amplifier  $f_{\text{GBW}}$  should be greater than 980 MHz and 1.3 GHz for a settling accuracy of 0.25 % and 0.033%, respectively.

TABLE I  
OPERATING CONDITIONS OF THE INTEGRATORS

Integrator	Load capacitance	$\beta$
1	0.7 pF	0.492
2	1.75 pF	0.195
3	1.1 pF	0.418
4	1.5 pF	0.215

Assuming that the system settles properly within the integrating phase, the settling error is ultimately determined by the factor  $\beta A_{v0}$ . For a settling error below 0.1 %,  $\beta A_{v0}$  must be greater than 60 dB; hence for  $\beta$  around 0.2 (-14 dB),  $A_{v0}$  must be greater than 74 dB for good settling performance. These performances were verified by using MATLAB behavioral models.

Another effect that increases the settling error is the switch resistance. In the previous analysis it was assumed that the input signal was a perfect pulse, but the switch resistance and the integrating capacitor filter out the high frequency components of the input signal leading to an equivalent quasi-exponential input signal. This effect increases both the time for slew and the time for settling. The settling time is determined by the RC time constant of the switches and performance metrics of the amplifier (slew rate,  $\omega_{\text{GBW}}$  and phase margin) [7].

### III. AMPLIFIER DESIGN

High gain amplifiers use cascode and multi-stage architectures, low bias currents and long channel devices, whereas high bandwidth amplifiers use single-stage architectures, high bias currents and short channel devices [5]. Two approaches for designing a high gain amplifier are cascode or vertical approach and cascode or horizontal approach. The signal swing in cascode amplifiers is constrained by the power supply voltage, which is a problem for low voltage designs. In cascaded amplifiers, each amplifier stage contributes a pole. Traditional Miller compensation schemes trade bandwidth for stability. The No Capacitor Feed Forward (NCF) compensation scheme [10] has been

proposed to overcome the limitations of Miller compensation schemes. The block diagram of the compensation scheme is shown in Fig. 2, where  $g_{mi}$  is the transconductance,  $r_{oi}$  is the output resistance and  $C_i$  is the total capacitance of  $i$ th stage.

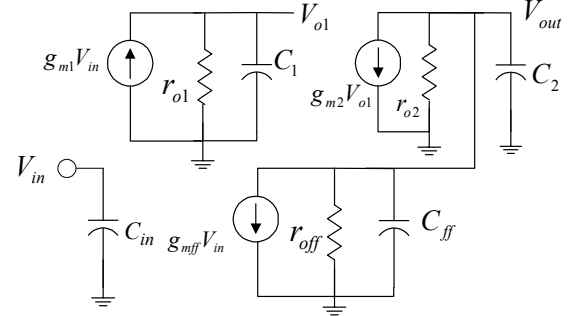


Fig. 2. Block diagram of NCFF compensation scheme

A feedforward path, which has the same phase shift as the direct path, produces a left half plane (LHP) zero. The positive phase shift of LHP zero is used to cancel the negative phase shift of pole, resulting in a good phase margin. This scheme shows a great improvement in bandwidth, along with a high gain and good phase margin. The compensation scheme also results in lesser area because of the absence of compensation capacitors. One of the main problems in this scheme is the imperfect cancellation of poles and zeros. The pole-zero mismatch results due to process, voltage and temperature (PVT) variations and introduces a high frequency pole-zero doublet that might affect the settling behavior. This effect is described in the following subsection.

The settling time of the SC integrator shown in Fig. 1 is affected by the presence of pole-zero doublet in the amplifier response [8] and the pulse response is given by

$$V_{\text{out}}(t) = V_{\text{in}} \left( \frac{-\frac{C_a}{C_f}}{1 + \frac{1}{\beta A_{v0}}} \right) \left( 1 - k_1 e^{-\beta \omega_{\text{GBW}} t} + k_2 e^{-\left(\frac{t}{\tau_2}\right)} \right) + V_o(t_0) \quad (4)$$

$$k_2 \cong \frac{\omega_z - \omega_p}{\omega_{\text{GBW}}}$$

$$\omega_p, \omega_z \rightarrow \text{Pole - zero doublet}, \tau_2 \cong \frac{1}{\omega_z}, k_1 \cong 1$$

As compared to (2), both the settling time and settling accuracy are affected by the pole-zero doublet. The effect of the extra term on settling time can be reduced by increasing the frequency of the zero, which causes the exponential term to decay very fast. The settling error can also be reduced by increasing the amplifier's  $\omega_{\text{GBW}}$  (which occurs in the denominator of  $k_2$ ), which is easily achieved with the proposed compensation scheme.

The amplifier shown in Fig. 2 consists of two stages in cascade with a feedforward stage used for compensation; the realization is shown in Fig. 3. To meet the requirements for best settling and stability, the first stage should have high gain for better accuracy. The second and feedforward stages should have medium gain. The first stage is implemented using a telescopic cascode amplifier and the second stage is a simple

differential amplifier [9]. As compared to the implementation in [10], the feedforward stage has been changed from a single differential pair to a cascode amplifier. Without M6 in the feedforward stage, the parasitic gate to drain capacitance  $C_{GD5}$  of M5 is in parallel with the feedback capacitor,  $C_f$  in Fig. 1, of a SC amplifier in closed loop operation. This changes the effective feedback capacitor to  $C_f + C_{GD5}$ . Since  $C_{GD5}$  is not very well controlled, it is difficult to accurately account for it when the capacitors are selected for coefficient implementation. A cascode amplifier in the feedforward path shields the gate-to-drain parasitic capacitance and gives a more accurate feedback factor. The transistor dimensions and bias conditions are given in Table II; the bias currents used are:  $I_{b1} = 100 \mu\text{A}$ ,  $I_{b2} = 1.25 \text{ mA}$  and  $I_{bff} = 3.25 \text{ mA}$ .

The open loop DC gain, poles and zero of the amplifier are given by (5)-(8).  $A_1$  is the gain of the first stage telescopic cascode amplifier,  $A_2$  is the gain of the second stage differential pair,  $A_{ff}$  is the gain of the feedforward cascode amplifier,  $g_{m,i}$  is the transconductance and  $r_{ds,i}$  is the drain-to-source resistance of  $i$ th transistor

$$A_v = A_1 A_2 + A_{ff} \quad (5)$$

$$\omega_{p1} \cong -\frac{g_{m2} r_{ds2} r_{ds1} \parallel g_{m3} r_{ds3} r_{ds4}}{C_{gs7}} \quad (6)$$

$$\omega_{p2} \cong -\frac{r_{ds7} \parallel r_{ds8} \parallel g_{m6} r_{ds6} r_{ds5}}{C_L} \quad (7)$$

$$\omega_z \cong -\frac{g_{m1}}{C_{gs7}} \left( \frac{g_{m7}}{g_{m5}} \right) \quad (8)$$

Minimum transistor length was used in M7 and M8 to limit the amplifier's output resistance such that  $\omega_{p2}$  is placed at high frequency - around  $2\pi \times 160 \text{ Mrad/sec}$ . The low frequency voltage gain  $A_2$  is around 20-25 dB. The locations of the first pole, second pole and the LHP zero are at 174 kHz, 162 MHz and 160 MHz, respectively. The performance metrics of the amplifier (simulation results) are summarized in Table III and are compared with amplifiers designed in the same technology. The reported performance in [11] is from measurement results. The transient response was simulated for the amplifier with the worst case feedback factor and process parameters were varied to cause mismatch in the location of pole-zero doublet. The plot of the error in the final settling value with respect to the pole-zero mismatch for the amplifier with a 100 MHz clock is shown in Fig. 4. In (3), the error is the addition of a positive term (GBW effect) and a negative term (pole-zero mismatch effect), which leads to the error being both positive and negative with pole-zero mismatch. Mismatches in the pole-zero doublet can tolerate around 33% mismatch for 0.01% error at the end of the integrating clock phase.

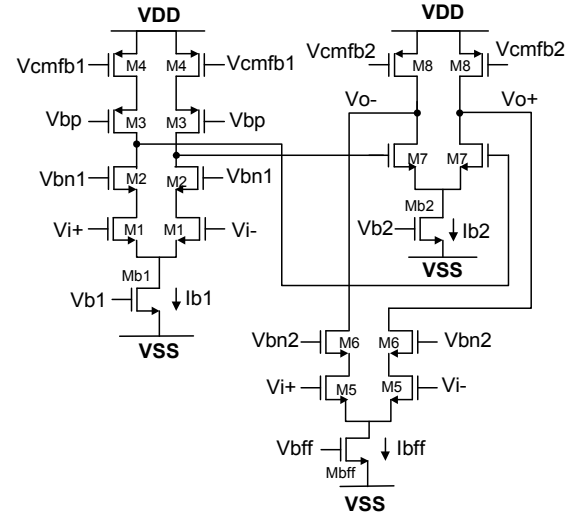


Fig. 3. Schematic of amplifier with NCF compensation

TABLE II  
TRANSISTOR DIMENSIONS AND BIAS CURRENTS

Transistor	W/L ( $\mu\text{m}/\mu\text{m}$ )	Transistor	W/L ( $\mu\text{m}/\mu\text{m}$ )
M1, M2	30/0.4	M8	150/0.4
M3, M4	45/0.6	M9	10/0.8
M5, M6	400/0.4	Mb1, Mb2	80/0.8
M7	200/0.4	Mbff	400/0.8

TABLE III  
SUMMARY AND COMPARISON OF AMPLIFIER PERFORMANCE

PARAMETERS	Ref [4]	Ref [11]	This work
DC gain	61 dB	56 dB	80 dB
$f_{GBW}$	430 MHz	600 MHz	1.4 GHz
Phase margin	61°	50°	62°
DC Current	9 mA	10.3 mA	4.6 mA
0.1% settling time	N/A	5 ns	2 ns
Input noise spectral density	N/A	N/A	3.5 $\text{nV}/(\text{Hz})^{1/2}$

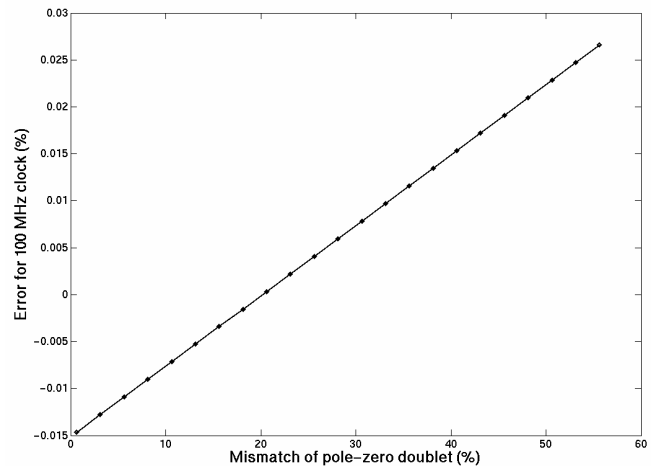


Fig. 4. Settling error vs pole-zero mismatch of amplifier for 100 MHz clock

#### IV. MODULATOR DESIGN

The architecture used for the modulator's implementation is a fourth order cascade of resonators in feedback (CRFB) [6]. The center frequency is located at  $\frac{1}{4}$  of the sampling frequency, for ease of digital demodulation. The coefficients are optimized based on tradeoff between signal swing in the internal nodes, capacitance spread and the maximum SNR attainable with stable operation. The value of capacitor in the first stage is important as its  $kT/C$  noise contribution dominates the overall noise performance. The out of band gain of the noise transfer function (NTF) is an important parameter for stability; in this design, this parameter is chosen to be 1.5, giving some margin for PVT variations. Simulations were done in Simulink and Matlab to verify the stability of the architecture over typical component variations. The block diagram of the architecture is shown in Fig. 5 and the optimized coefficients used in the modulator implementation are given in Table IV. Switches are implemented using only NMOS transistors with a boosted clock voltage to reduce the switch resistance. The comparator is a two-stage structure, with a low gain first stage followed by a latch. A single-bit DAC is used to feedback the digital output; the reference voltage used was 0.25 V.

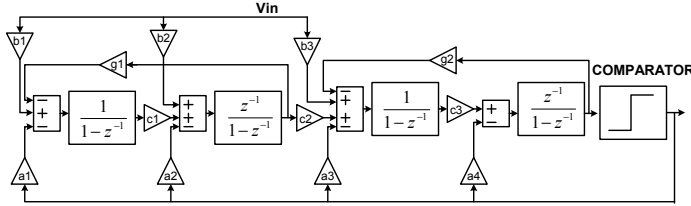


Fig. 5. Block diagram of CRFB architecture

TABLE IV  
COEFFICIENT VALUES FOR CRFB ARCHITECTURE

Coefficients	Value
a1,a2,a3,a4	-0.3122, 0, 0.5316, 0.5316
b1,b2,b3	-0.25, 0.25, 0.125
c1,c2,c3	1, 1, 1
g1,g2	2, 2

#### V. MODULATOR EXPERIMENTAL RESULTS

The chip was fabricated in the TSMC 0.35 $\mu$ m CMOS technology through the MOSIS educational program. Common centroid and interdigitization techniques were used in the layout to minimize mismatches in the design. The chip micrograph of the bandpass  $\Sigma\Delta$  modulator is shown in Fig. 6. It occupies an area of 1.25 mm<sup>2</sup>. The bandpass modulator was characterized by directly injecting the output digital bit stream into a spectrum analyzer. The clock frequency is at 92 MHz and the IF signal is at 23 MHz. The NTF of the modulator measured by grounding the inputs is shown in Fig. 7. The noise floor of the modulator is at -127 dB. This level is determined not only by the noise shaping of the sigma-delta modulator and thermal noise of the transistors, but also the noise added to the digital levels (from noisy supply voltages) since the output is directly injected into the spectrum analyzer. The output spectrum with the two-tone input signal at 23 MHz is shown in Fig. 8. Noise level increases mainly due to the

noise contribution of the signal generators used. The two-tone test for signals 200 kHz apart in the band (22.9 MHz and 23.1 MHz) are shown in Fig. 9. IM3 is less than -58 dB for two-tone input signals, each at -11 dB<sub>r</sub> (normalized with respect to the reference voltage of 0.25 V). The peak SNR of the modulator was 80 dB and 54 dB for bandwidth of 270 KHz and 3.84 MHz, respectively. The SNR for various values of input signal is shown in Fig. 10. The performance of the modulator is summarized in Table V and is compared with Ref [4], which was designed in the same technology for similar application.

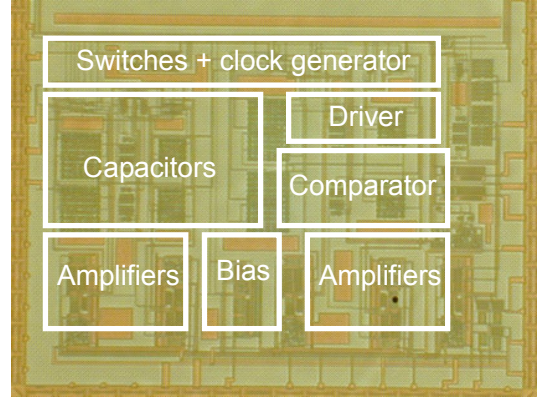


Fig. 6. Chip microphotograph

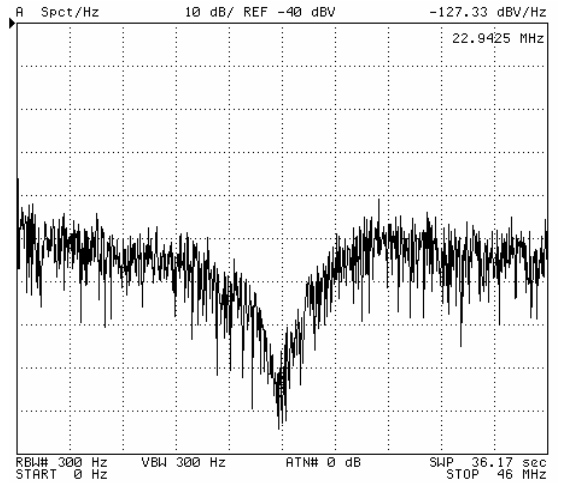


Fig. 7. Measured noise transfer function of ADC

The clock frequency for implementation in [6], which is a CRFB architecture, is 42.8 MHz. By using the proposed amplifier in a similar architecture, the clock frequency can be increased to 92 MHz with lesser power consumption. The clock frequency can further be doubled to 180 MHz by using techniques like two-path architecture or double sampling architectures. Simulations showed that the maximum frequency of operation is further affected by the switch resistance as well. The settling time of the SC integrator increases by 2-3 times the time constant associated with the switches ( $R_{\text{switch}}C$ ). From simulations, the worst case value of product of switch resistance and capacitance,  $R_{\text{switch}}C$  is 0.6 ns. Therefore, the delay due to switch resistance is around 1.8 ns and the amplifier starts to react after this delay. The worst case slew rate in the integration phase is around 1 V/ns,

resulting in 1 ns slew phase for a maximum differential voltage of 1 V (limited by current at amplifier output stage and load capacitor) and after that 2 ns for linear settling phase (limited by amplifier GBW, refer to (4)). The worst case value of total settling time for SC integrator is 4.8 ns. This is not sufficient for the operation of the modulator at 100 MHz, where the integration period was around 4.6 ns (taking into account the non-overlapping time of the clocks). Also, the linearity of the switches degrades for frequencies greater than 92 MHz and limits the overall ADC performance.

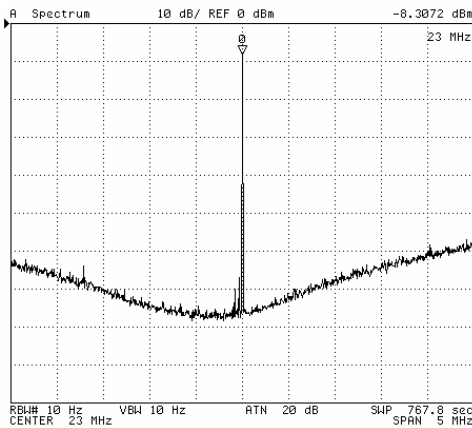


Fig. 8. Output spectrum of ADC for 5 MHz span

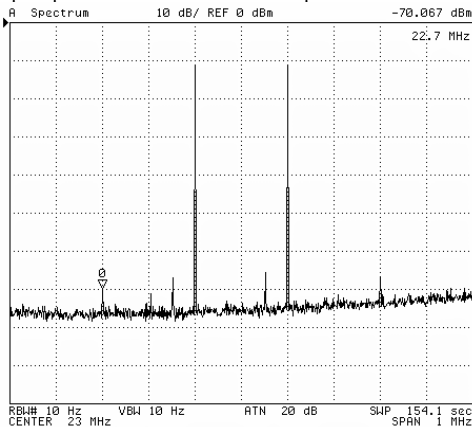


Fig. 9. Two tone IMD test for -11 dBm input signal

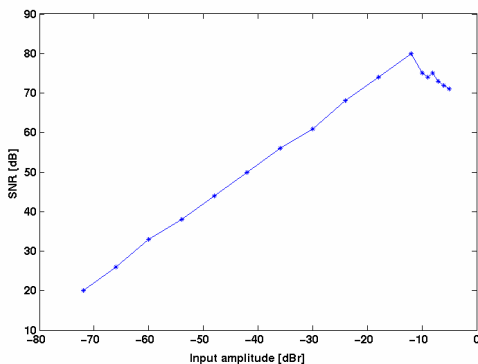


Fig. 10. Plot of SNR vs input amplitude for 270 kHz bandwidth

## VI. CONCLUSIONS

The performance limitations of a switched capacitor integrator were analyzed and it was shown that an amplifier with high gain and GBW is required for accurate and fast

response. A feedforward compensation scheme was used to design a high gain and fast settling OTA in 0.35  $\mu\text{m}$  CMOS technology. The amplifier's performance was verified by using it in a fourth order bandpass sigma-delta ADC. It was also found that the main limitation to the system's speed was the switch resistance.

## ACKNOWLEDGMENTS

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TABLE V  
PERFORMANCE SUMMARY OF THE BANDPASS  $\Sigma\Delta$  ADC

PARAMETERS	Ref [4]	This work
Peak SNR @ 270 KHz	78 dB	80 dB
Peak SNR @ 3.84 MHz	48 dB	54 dB
IM3 @ 2-tones -11 dBm	N/A	-58 dB
Sampling frequency	80 MHz	92 MHz
Number of Opamps	1 (time sharing)	4
Power consumption	38 mW	47.5 mW
Core area	1.0 mm <sup>2</sup>	1.25 mm <sup>2</sup>
Supply voltage	3 V	$\pm 1.25\text{V}$
Technology (CMOS)	0.35 $\mu\text{m}$	0.35 $\mu\text{m}$

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