



Series/Parallel Time-Multiplexed Switched-Capacitor Filters with Programmability Based on Non-Uniform Sampling

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Received October 22, 2004; Accepted May 9, 2005

Abstract. This paper presents an improved scheme for programmable time-multiplexed (TM) switched-capacitor (SC) filters. The proposed approach uses a novel sampling technique, which eliminates the need for resolution/area tradeoffs. The programmability of each processing channel is based on the use of non-uniform clock signals with noise-shaped sampling energy. No capacitor values are modified for programming frequency response parameters and, hence, the performance of the TM SC filter is not sacrificed for programmability. Such a sampling technique not only leads to an accurate frequency response control, but also allows the design procedures and the resulting SC circuit implementation to be simplified. A test-chip including a programmable second-order TM SC filter with a multiplexing order of four, which operates in series or in parallel mode, was fabricated in conventional CMOS technology. Measurement results demonstrate the effectiveness and versatility of the proposed technique.

Key Words: switched-capacitor filters, time-division multiplexing, programmability, non-uniform sampling, noise-shaping modulation

1. Introduction

Switched-capacitor (SC) techniques are a very popular approach for the implementation of high-precision analog filtering functions. Conventional design approaches for SC filters require a number of amplifiers that is proportional to the order of the realized transfer function. Time-division multiplexing (TDM) techniques have traditionally been used to reduce amplifier count in several applications [1–10]. TDM techniques involve the presence of N processing channels (N is referred to as the multiplexing order). The overall repetition period NT_s (where $T_s = 1/f_s$ is the period of the master clock signal) is divided into N time slots. Each time slot has a duration equal to T_s and is devoted to a single processing channel. Hence, the effective sampling frequency for each channel coincides with f_s/N . In this paper, circuits based on TDM will be referred to as time-multiplexed (TM) circuits.

From a general point of view, two different operating modes can be distinguished in a TM SC circuit, namely, series and parallel operations. Figure 1(a) shows the basic principle of series TM operation. The input signal is only sampled in the time period P_1 . After processing this input sample, the output samples are forced to successively recirculate through the circuit, which realizes a different transfer function, $H_i(z)$, in

each time interval P_i ($1 \leq i \leq N$). A sample-and-hold (S/H) block is provided at the output of the SC filter to ensure a stable input signal for the SC section at any period P_i . Thus, the complete circuit transfer function coincides with the product of the transfer functions corresponding to the individual channels. The filter output is only valid during the time interval P_1 . The most typical application of series TM operation consists in realizing high-order or/and high-selectivity transfer functions by using lower-order circuits [1–5].

In parallel TM operation [Fig. 1(b)], the input signal is sampled at every period P_i , and the SC circuit realizes a different transfer function, $H_i(z)$, in each time interval P_i [i.e., $V_{o,i}(z) = H_i(z) \cdot V_{in}(z)$]. While the i -th channel is active during P_i , the rest of the channels are inactive during this interval. The most typical application of parallel TM operation is filter bank implementation [6–10].

Nevertheless, a main drawback arises associated to traditional TM systems, namely a reduced dynamic range. The loss of dynamic range occurs mainly due to two effects. First, in systems where some response parameters have to be tuned depending on the specific application or, simply, where the specifications are not well known in advance, a certain degree of programmability must be provided. Conventional SC techniques use digitally programmable capacitor arrays (DPCAs)

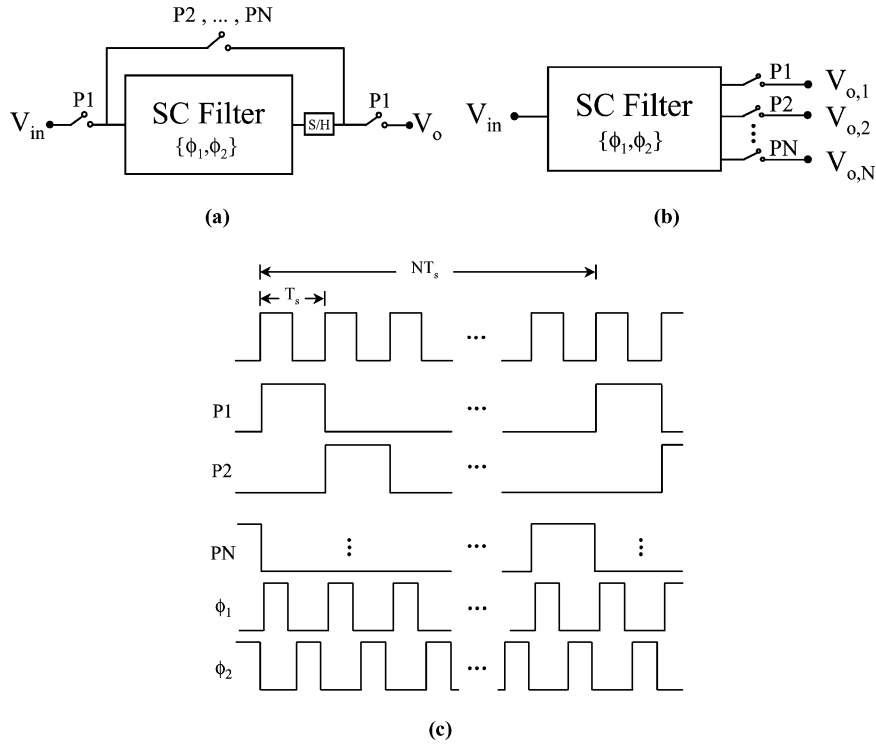


Fig. 1. Block diagram of a series (a) and a parallel (b) TM SC circuit, and (c) clock signals.

to modify some magnitudes of the response. However, the variability of capacitor values precludes the optimum capacitance scaling for maximum signal swing, thus limiting the achievable dynamic range. Second, in TM SC filters, different channels generally have different offset transfer functions [6, 9]. The presence of any offset difference between channels reduces the effective available output swing, thereby further decreasing the dynamic range. As a consequence, ways to properly program the frequency response of TM SC circuits while still maintaining adequate performance must be developed.

A technique that uses periodical non-uniform sampling (PNS) to achieve wide tunability range and resolution in the frequency response of SC circuits, while minimizing capacitance spread and dynamic range degradation, has been proposed [11]. This technique is based on digitally controlling the effective sampling frequency $f_{s,eff}$ and, hence, the equivalent resistance of appropriate SC structures, whose operating clock phases are generated from a periodical non-uniform (PN) clock signal. Figure 2 shows a PN clock signal ϕ_{PN} derived from a continuous master clock signal ϕ_s . The PN clock signal is periodically activated during p_j cycles in the j -th time interval within a sequence of M time intervals mT_s ($j = 1, 2, \dots, M$ and $1 \leq p_j \leq m$). The number of active pulses p_j of the signal ϕ_{PN} may be different in successive time intervals mT_s . Therefore, the pulse sequence has an overall repetition period equal to MmT_s .

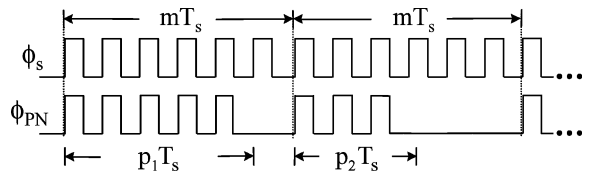


Fig. 2. Periodical non-uniform clock signal ϕ_{PN} derived from a master clock signal ϕ_s ($m = 6$, $p_1 = 5$, and $p_2 = 3$).

Assuming that the sampling rate is much higher than the signal bandwidth of interest, the equivalent number, p_{eq} , of active pulses of ϕ_{PN} in an interval mT_s can be expressed as $p_{eq} = (1/M) \cdot \sum_{j=1}^M p_j$. When all SC branches in a circuit are operated by clock phases derived from the same clock signal ϕ_{PN} , it is possible to realize frequency scaling in the circuit response by programming their effective sampling frequency, which turns out to be equal to $p_{eq}/(mT_s)$. When this operating scheme is applied to TM SC circuits, neither the voltage swing at any node nor the dc output offset due to the input offset voltage of the amplifiers are affected by programmability and, hence, the dynamic range loss can be avoided [11]. A limiting factor of this method is that the allowed signal bandwidth depends on the programmability range and resolution required, as will be shown in more detail in next Section.

In this paper, a modified version of the PNS technique well suited to TM SC filters is presented. The proposed solution is based on using non-uniform clock signals

generated by means of a pulse-width modulated waveform whose duty cycle changes aperiodically under the control of a noise-shaping feedback coder. In this way, the periodicity of the operating clock signals is randomized, and the impact on the allowed signal bandwidth is kept to a minimum. The rest of the paper has been organized as follows. In Section 2, the application of the PNS approach to series/parallel TM operating modes is discussed, and the improved technique based on the use of noise-shaping coders is presented. Section 3 deals with the design and the circuit implementation of a series/parallel TM second-order SC filter ($N = 4$) based on the proposed methodology. The frequency response type (low-pass, band-pass, or high-pass) of each channel is selected separately. The programmability in the central/cutoff frequency of any single channel is achieved by controlling the value of its effective sampling frequency. Experimental results obtained from a test-chip, that verify the versatility of the proposed approach,

are shown in Section 4. Finally, Section 5 draws some conclusions.

2. Time-Multiplexed SC Circuits with Non-Uniform Sampling

2.1. Series/Parallel TM PNS-Programmable SC Circuits

Figure 3 shows a two-channel series/parallel TM damped SC integrator programmable by PNS, along with its non-uniform clock signals ($N = 2, M = 1$). A S/H block driven by clock signal $P2$ was connected to the terminal v_{o2} for better uniformity between the two channels. The parallel TM operation of the damped SC integrator is as follows. Switches $S1$ and $S2$ are permanently on and off, respectively, whereas switches $P_i (i = 1, 2)$ are activated, sequentially, during the

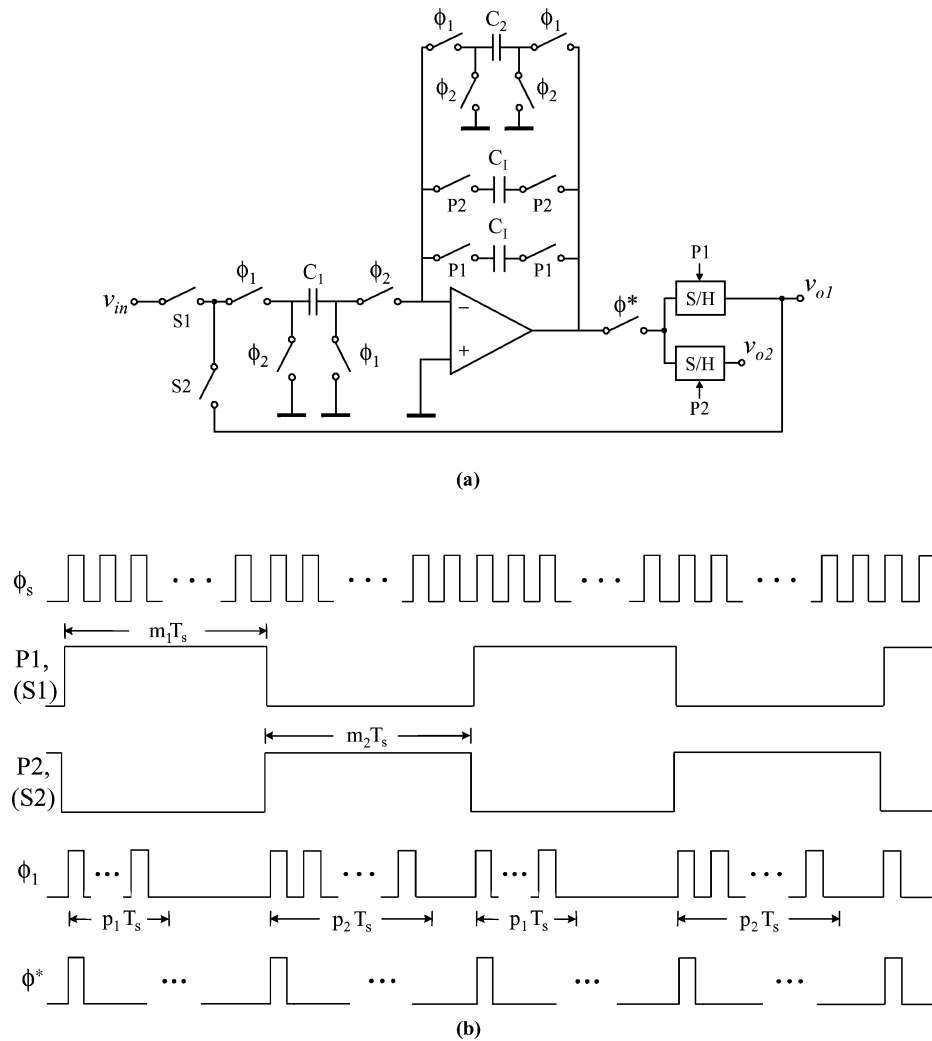


Fig. 3. (a) Series/parallel TM SC damped integrator ($N = 2$). (b) Clock signals for PNS operation. The waveforms for signals $S1$ and $S2$ refer only to series TM mode.

corresponding time interval $m_i T_s$. Notice that, in general, m_i can be different for the two time intervals. Thus, the output samples of every channel are stored in the corresponding integrating feedback capacitor C_I . The cutoff frequency of the i -th channel can be approximated by [11]

$$\omega_{oi,\text{PNS}} \cong \frac{1 - a^{p_{\text{eq},i}}}{m_1 + m_2} \cdot \frac{1}{T_s} \quad (1)$$

where a is equal to $C_I/(C_I + C_2)$ and $p_{\text{eq},i}$ refers to the equivalent number of active pulses of the i -th channel. In common practical cases, C_2 is set much less than C_I and, therefore, a is nearly equal to unit. In this case, $\omega_{oi,\text{PNS}}$ turns out to be equal to $\omega_o \cdot (p_{\text{eq},i}/m)$, where ω_o is the cutoff frequency of the damped SC integrator operating with conventional uniform sampling at f_s [i.e., $\omega_o = (1 - a)f_s$] and $m = m_1 + m_2$.

In series TM operation, switches S_i are controlled by the same clock signals as their P_i counterparts and, hence, any input signal sample is successively processed according to the transfer function realized by each of the two channels. Thus, the cutoff frequency of the i -th channel is still given by Eq. (1), and a global transfer function that coincides with the product of the individual transfer functions of the two channels, is implemented.

Equation (1) indicates that the value of $\omega_{oi,\text{PNS}}$ can be programmed by controlling the number of active pulses $p_{\text{eq},i}$, i.e., by varying the effective sampling frequency of each channel $f_{s,\text{eff},i}$. Moreover, the charge transfer in any active clock phase is the same as in the case of traditional uniform sampling and, hence, the passband gain is not modified. Therefore, frequency scaling in the response of both channels in the series/parallel TM damped SC integrator can be programmed by PNS. The above result can be extended to any value of M and to any high-order TM SC filter structure. However, since the operating phases are derived from PN clock signals, their overall repetition period leads to an allowed signal bandwidth BW expressed as

$$BW = \frac{f_s/2}{\sum_{i=1}^N m_i M_i} \quad (2)$$

With the same programmability resolution, i.e., with the same values of $M_i (=M)$ and $m_i (=m)$, respectively, for all channels, (2) reduces to $BW = f_s/(2MNm)$. For coarse tuning ($M = 1$), the maximum allowed frequency is generally not a very restrictive limit. However, when a fine resolution is required, the value of M should be much larger than unit, which implies that f_s must be increased by a factor of M in order to maintain the same BW as for coarse tuning.

The above problem can be greatly mitigated by randomizing the overall repetition period of the operating

clock signals, while still maintaining the correct value of $p_{\text{eq},i}$. In the past, noise-shaping techniques have been proposed to reduce spurious output tones in fractional- N frequency synthesizers [12], which is mainly caused by the periodicity in the divider modulus control. This premise led us to consider noise shaping techniques to provide operating clock phases with a better spectral content as compared to the case of the above mentioned PNS scheme. In particular, we investigated the use of noise-shaping feedback coders to control the number of active clock pulses, with the purpose of providing high-resolution programmability without limiting the allowed signal bandwidth.

2.2. Proposed Non-Uniform Sampling Scheme

The periodicity of PNS-based clock signals can be reduced by masking a continuous clock signal with a square waveform whose duty cycle is modulated by means of noise-shaping techniques. A programmable clock signal generator according to this approach varies the number of active clock pulses present in successive time intervals mT_s by using the output of a noise-shaping coder. In the following analysis, for simplicity, we refer to the case of a single processing channel ($N = 1$), but all concepts are easily extended to the case of $N > 1$.

The topology of a conventional noise-shaping feedback coder is shown in Fig. 4. It consists of two main blocks, namely a coarse quantizer and a low-pass finite-impulse-response filter $H(z)$ [13]. Using a linear model for the quantizer, the z -transforms $Y(z)$, $X(z)$, and $E(z)$ of the coder output sequence $y(n)$, the input sequence $x(n)$, and the quantizer error sequence $e(n)$, respectively (where n is an integer denoting the sampling instants), are related by the following equation:

$$Y(z) = X(z) + [H(z) - 1] \cdot E(z) \quad (3)$$

and the z -transform $\hat{E}(z)$ of the output error sequence $\hat{e}(n) = y(n) - x(n)$ is related to $E(z)$ by

$$\frac{\hat{E}(z)}{E(z)} = H(z) - 1 = C(z) \quad (4)$$

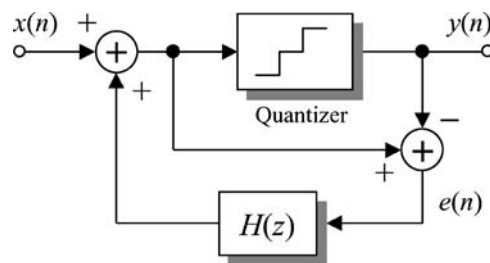


Fig. 4. Block diagram of a noise-shaping feedback coder.

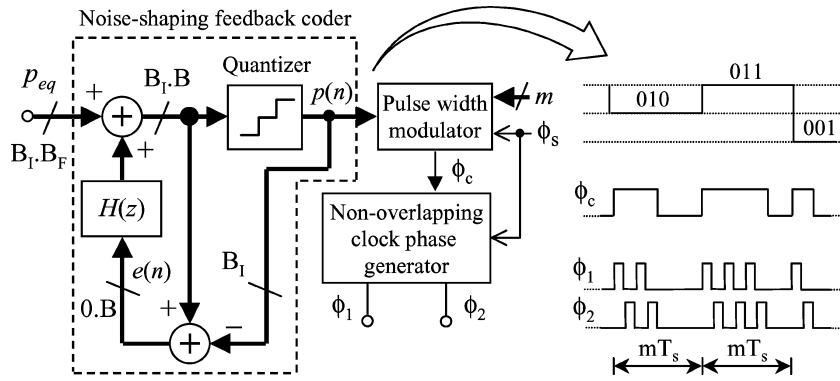


Fig. 5. Programmable clock signal generator based on noise-shaping coder control.

If $H(z)$ has unity dc gain property, $C(z)$ turns out to have a high-pass response with a zero at dc. Hence, the coder shown in Fig. 4 shapes the power spectrum of the noise sequence $e(n)$, by moving the quantization error energy towards high frequencies. This result implies that the average value of $y(n)$ equals the average value of $x(n)$. Thus, the output $y(n)$ contains all the information carried by $x(n)$ and can be seen as its digitally coded version. The circuit in Fig. 4 is algebraically equivalent to a sigma-delta coder, but has the practical advantage that it is very well suited to digital implementations, where no coefficient mismatches occur.

One possible all-digital implementation of the above programmable clock generator based on noise-shaping coder control is shown in Fig. 5. The coder sampling interval is equal to mT_s . The input signal p_{eq} is a constant binary word with B_I integer and B_F fractional bits (i.e., $p_{eq} = B_I.B_F$ represents the desired equivalent number of active pulses of the non-overlapping clock phases ϕ_1 and ϕ_2 during one sampling interval). The quantizer produces a multilevel digital signal $p(n)$, whose average value equals p_{eq} . The coder output is used as the control input of a digital pulse width modulator. This block is basically composed by one loadable counter and one digital comparator. The period of the pulse-width-modulated (PWM) signal ϕ_c is equal to mT_s , and its pulse width during the n -th interval mT_s is equal to $p(n) \cdot T_s$. Therefore, the average duty cycle of the PWM signal is made equal to p_{eq}/m . The signal ϕ_c , in turn, masks the output of a non-overlapping clock phase generator so as to obtain the appropriate active pulses of a non-uniform clock signal ϕ_N (i.e., ϕ_1 and ϕ_2) from the continuous master clock signal ϕ_s . Thus, the average number of active pulses over a time interval mT_s is equal to p_{eq} .

The advantages of the above encoding method are best demonstrated by comparison with the periodical pulse-width modulation technique used in the PNS ap-

proach. For instance, consider the PNS waveform in Fig. 6(a) with $m = 4$, $M = 4$, $p_1 = p_2 = p_3 = 2$, and $p_4 = 3$, which can be used to encode the value $p_{eq} = 2.25$ by masking a continuous clock signal ϕ_s over $m \times M = 16$ cycles. Most of the harmonic energy of this waveform is concentrated at $f_s/(M \cdot m)$. By using noise-shaping feedback coding which, in this case, gives rise to the waveform conceptually illustrated in Fig. 6(b) for $2Mm = 32$ clock cycles, we can obtain the same value of p_{eq} , while taking advantage of the frequency characteristic of non-periodic duty-cycle modulation. Figures 6(c) and (d) show the Fourier coefficients corresponding to the PNS-based clock signal obtained from the waveform of Fig. 6(a) and to the noise-shaping based non-uniform clock signal corresponding to the waveform in Fig. 6(b), respectively (the two clock signals have the same sampling rate). It is apparent that noise shaping eliminates the unwanted tones at integer multiples of $f_s/(M \cdot m)$ (i.e., the tones at $f = k \times f_s/(M \cdot m)$, k being an integer different from M) associated with periodical non-uniform clock signals. Since the spectrum repetition frequency is now $1/(mT_s)$, a BW increase by a factor of M is achieved with respect to PNS.

Therefore, by using noise-shaping techniques, high programmability resolution can be achieved in TM SC circuits, whereas the minimum master clock frequency to avoid aliasing distortion is still given by the relationship

$$2 \cdot BW \cdot N \cdot m < f_s \tag{5}$$

Finally, it should be pointed out that, as digital circuits benefit from technology scaling, the need for N different programmable non-uniform sampling clock generators does not represent a great disadvantage in modern integrated circuits.

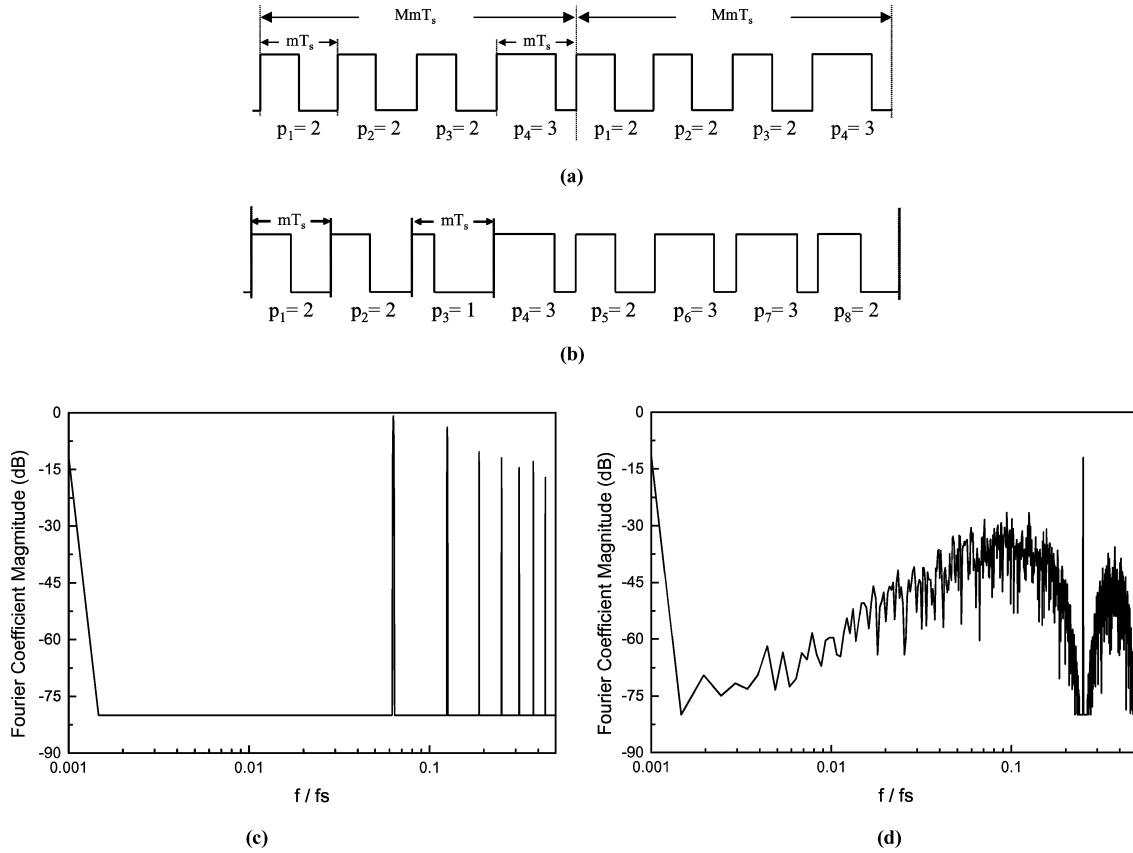


Fig. 6. Examples of (a) a periodic pulse-width modulated signal and (b) a non-periodic duty-cycle modulated signal, which encode the same value $p_{eq} = 2.25$. (c) Spectral coefficients demonstrating the advantages of noise-shaping based non-uniform clock signals over their periodical non-uniform counterparts.

3. Design and Implementation of a Noise-Shaping Based Series/Parallel Second-Order Programmable TM SC Filter

In order to demonstrate the effectiveness of the proposed sampling strategy in the design of programmable TM SC circuits, the second-order TM SC filter ($N = 4$) shown in Fig. 7 was designed. The filter can provide low-pass (LP), band-pass (BP), and high-pass (HP) responses, by enabling appropriate signal paths through respective switches. The TM operating mode is controlled by means of switches P_i and S_i ($i = 1$ to 4). Every set of switches P_i corresponds to one of the four channels when the SC circuit operates in parallel TM mode (obviously, when the circuit acts as a single-channel second-order filter, just one set of switches P_i is permanently active, while the rest of them are in the off state). Switches denoted as S_i only operate in series TM mode, so as to make the samples recirculate sequentially through the different channels. In any other operating mode (such as parallel TM and single-channel stand-alone filter modes), switch S_1 is permanently in the on state, while the rest of switches S_i are turned off.

The cutoff/central frequency, f_{oi} , of the i -th channel is controlled with the non-uniform clock phases ϕ_1 and ϕ_2 , which are obtained from a programmable non-uniform clock signal generator based on the scheme in Fig. 5, while the passband gain and the quality factor Q will remain unchanged. With this approach, the following first-order expressions can be derived for the response parameters of the biquad section:

$$f_{oi} \cong \frac{p_{f,eq,i}}{2\pi mNT_s} \cdot \sqrt{\frac{AC}{D(B+F)}} \quad (6a)$$

$$Q \cong \frac{1}{F} \sqrt{\frac{AC(B+F)}{D}} \quad (6b)$$

where $p_{f,eq,i}$ refers to the average equivalent number of the active cycles of the i -th channel during the corresponding time interval mT_s .

By using (6), the circuit capacitor values $\{A, B, C, D, F\}$ were determined for satisfying the conditions $f_{oi} = 0.01 \times f_{s,eff,i}$ when $p_{f,eq,i} = 1$, and $Q = 0.707$. The rest of the capacitors, i.e., $\{G, H, I\}$, were determined so as to have unity gain of the filter in the

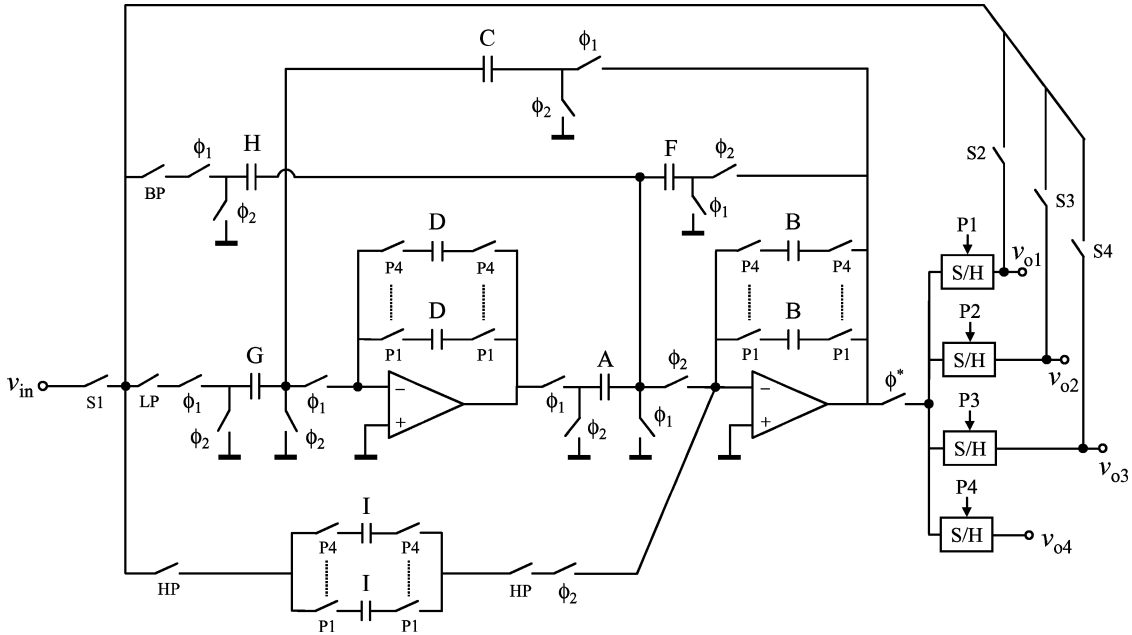


Fig. 7. Circuit schematic of the designed TM SC filter programmable by PNS with $N = 4$. Clock signals P_i and S_i ($i = 1$ to 4), as well as phases ϕ_1 (ϕ_2) and sampling phase ϕ^* , are an extension of the corresponding signals in Fig. 3.

pass band. After scaling the capacitor values for maximum signal swing at each node and for minimum silicon area, the values in Table 1 were obtained. The value of m was set to 8 for all channels, and the cut-off/central frequency is controlled by a 3.5-b number (i.e., 3 integer bits and 5 fractional bits were chosen for $p_{f,eq,i}$). The coder was designed by using a 3-b quantizer, which receives a 3.12-b input, and the transfer function $H(z) = 2z^{-1} - 0.5z^{-2} - 0.5z^{-3}$, which determines the programmability range of $p_{f,eq,i}$. Since the values of the quantizer error sequence $e(n)$ are comprised between 0 and 1, the values of the output of $H(z)$ lie in the range from -1 to 2. Therefore, the value of $p_{f,eq,i}$ should vary, ideally, from 2 to 7 (with a step of $1/32$) in order to prevent the quantizer from overloading. However, from simulation results, the variation of $p_{f,eq,i}$ can be in the range $1.5 \leq p_{f,eq,i} \leq 7$ without giving rise to loop instability. The sequence $e(n)$ is equal to the fractional part of the quantizer input sequence and, hence, no hardware subtractor is needed.

The described circuit, along with a digital section to provide the necessary clock signals (equivalent

gate count = 900), was fabricated in a double-poly two-metal $1.2\text{-}\mu\text{m}$ CMOS technology. Although this is not a very up-to-date technology, it gives accurate and reliable information about the benefits of the proposed sampling scheme. Figure 8 corresponds to a chip microphotograph of the fabricated circuit. The die size of the circuit portion including the TM biquad, four S&H blocks, and the logic section is about 2 mm^2 . The circuit was designed to operate with 3-V supply voltage and a master clock frequency $f_s = 1\text{ MHz}$. The operational amplifiers are implemented with a classical two-stage Miller compensated topology. Simulation results showed that the amplifier achieves an open-loop dc gain of 85 dB, a unity-gain frequency of 8 MHz, and a phase margin of 66° in the presence of a 20-pF load. Poly-to-poly capacitors were used for good linearity. Each capacitor was laid out to reside over a separate n -well region connected to ground. For better matching, dummy capacitors were also incorporated. Switches were implemented by complementary transistors, whose aspect ratios were set to $(W/L)_{\text{NMOS}} = 10\ \mu\text{m}/1.2\ \mu\text{m}$ and $(W/L)_{\text{PMOS}} = 30\ \mu\text{m}/1.2\ \mu\text{m}$. The S/H blocks in the circuit are based on a two-stage folded-cascode Miller-compensated amplifier connected in non-inverting unity-gain configuration. To extend the input common-mode range up to the rails, the input stage is based on parallel-connected complementary differential pairs. A single bias circuit is shared by all the amplifiers included in the TM SC biquad.

Table 1. Capacitor values (pF) for the SC filter in Fig. 7.

A	1.54	F	1.72
B	15.38	G	0.25
C	0.25	H	1.51
D	5.7	I	16.8

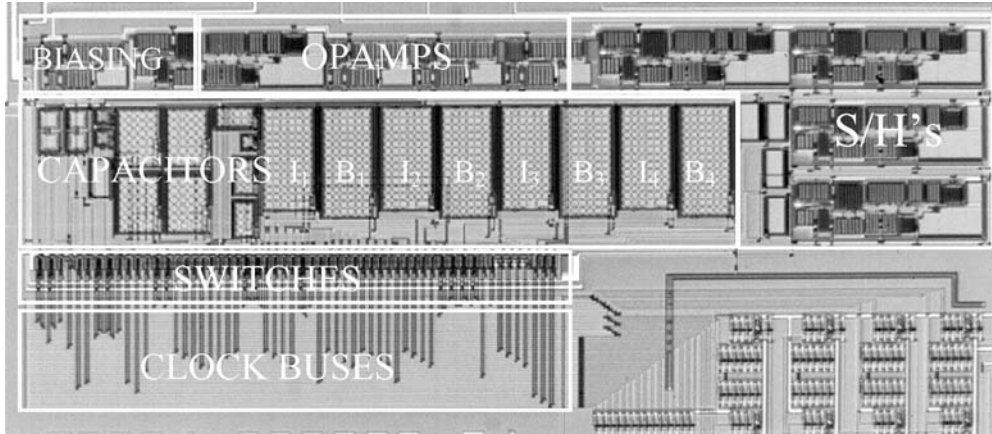


Fig. 8. Chip microphotograph of the fabricated second-order programmable TM SC filter.

4. Experimental Results

First of all, the programmable clock generator (PCG) was programmed to generate the required clock signals for 4-channel series TM operation of the SC biquad. Each channel was programmed to provide, separately, an identical LP response [$f_{oi} = 1.25$ kHz ($p_{f,eq,i} = 4$)]. In general, for l cascaded second-order sections with identical f_o , the cutoff frequency, f_{-3dB} , of the resulting filter is given by

$$f_{-3dB} \cong f_o \cdot [2^{1/l} - 1]^{1/4} \quad (7)$$

Therefore, for $l = 4$ and $f_{oi} = 1.25$ kHz, f_{-3dB} should be 824 Hz. Figure 9(a) depicts the experimental frequency responses. In this plot, the 2-nd order LP response corresponds to the output of the first channel (i.e., v_{o1} in Fig. 7), the 4-th order LP response is obtained at the output of the second channel (i.e., v_{o2} in Fig. 7), and so on. The measured 8-th order LP response (solid line), which corresponds to the response at the output of the 4-th channel (i.e., v_{o4}), is also compared in Fig. 9(a) to the simulated response (dotted line). As observed, a very good agreement is obtained between the measured and the simulated response.

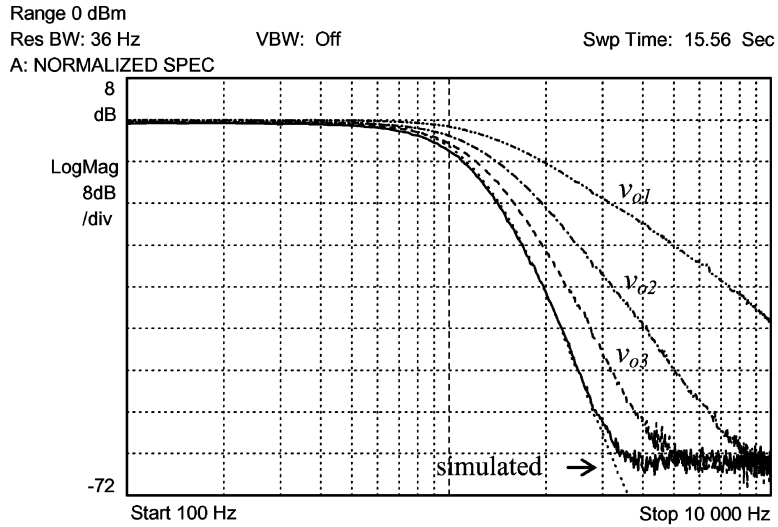
The PCG was subsequently programmed to obtain five different values of $p_{f,eq,i}$ from 3.9375 to 4.0625 (step = 1/32), and each channel was programmed to provide, separately, an identical LP response. Therefore, the cutoff frequency of each channel varies between 1230 and 1269 Hz with a step of about 10 Hz, which corresponds to a shift of 0.8%. The ensuing frequency responses measured at the output of the 4-th channel (cutoff frequency varying from 811 to 836 Hz) is shown in Fig. 9(b). The measured shift of f_{oi} and f_{-3dB} agree with the shift predicted by (6a) and (7), respectively. Moreover, the achieved bandwidth increase with respect to the original PNS approach (where

$BW = f_s/(2MmN) = 1/(2 \cdot 32 \cdot 8 \cdot 4)$ MHz \cong 488 Hz) is clear.

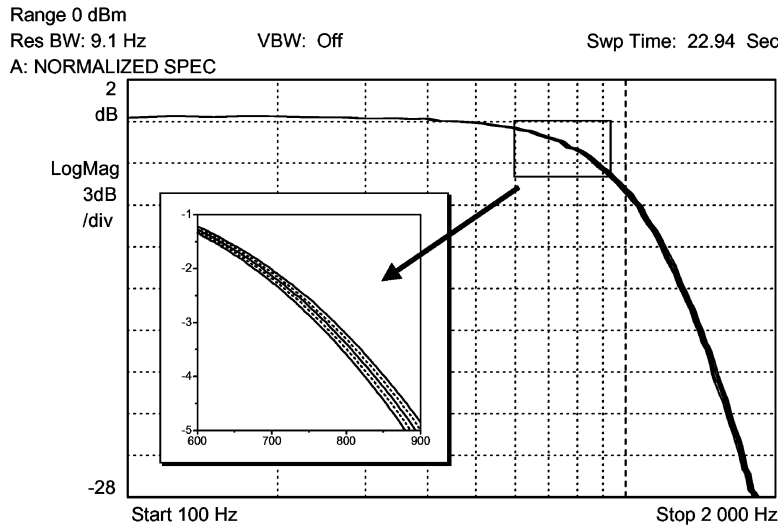
When applying a $2.5 \cdot V_{pp}$ input sinewave at $f_{oi}/6$, an almost constant total harmonic distortion (THD) of 0.5% was measured over the above mentioned programmability range, as a consequence of the fact that the voltage swing in any circuit node is not affected by programmability. The measured signal-to-noise ratio (SNR) was 74 dB. The SNR of the LP filter shows a slight decrease with increasing f_{oi} , due to the increased output noise. Indeed, the noise output spectrum has a shape very similar to that of the filter frequency response. The observed maximum total integrated output noise variation in the band up to $f_s/(2mN) = 15.625$ kHz was around $60 \mu\text{V}_{rms}$.

Next, as an application example of series TM operation, we consider an SC LP filter for potential use in a speech inversion scrambler. The purpose of an inversion scrambler is to prevent unauthorized “listening-in” on conversations. To this end, this device first splits the audio input signal into a high and a low frequency band (through adequate low-pass filtering), then inverts the frequency contents in the lower and in the higher band by means of respective modulators, and finally adds the two inverted bands to obtain the output signal. In order to provide greater protection, the scrambler dynamically selects the frequency, f_{split} , at which the input signal is split. Hence, the higher the resolution of f_{split} , the better the protection.

When SC techniques are used to implement the scrambler, f_{split} is set equal to the cutoff frequency of a high-order SC LP filter, and its value is changed by modifying the sampling frequency. However, if the sampling clock is realized by integer division of a fast master clock, only widely spaced sampling frequencies can be generated and, hence, the scrambler has a poor resolution. The programmability resolution can be increased by using a programmable dual-modulus divider or by



(a)



(b)

Fig. 9. Experimental LP frequency responses of the four channels in series TM operation. (a) The 8-th order LP response (solid line) can be compared to the simulated response (dotted line). (b) The index $p_{f,eq,i}$ is varied from 3.9375 to 4.0625 with a step of 1/32.

using DPCAs. However, the former approach is prone to spurious frequencies [12] and the latter degrades performance, as mentioned in the Introduction. By using the proposed non-uniform clock signal generator, quasi-continuous programmability is provided with no performance degradation. In particular, the TM SC filter in Fig. 7 can be programmed to provide the LP response required in the scrambler by cascading three identical LP stages and a notch stage. The latter is implemented by simultaneously enabling the LP and the HP path in the biquad section. Figure 10 illustrates the experimental 8th-order lower-band LP responses for speech scrambler filtering when $p_{f,eq,i}$ is set to 3.21875 ($f_{oi} = 1005$ Hz, $f_{split} = 500$ Hz) and to 3.84375 ($f_{oi} = 1200$ Hz, $f_{split} = 600$ Hz). Values for more than 170 split frequencies can be controlled by the proposed PCG.

There are several potential mechanisms associated with the operation of any TM circuit, which can lead to some loss of accuracy [5]. The most important cause of accuracy loss consists in the crosstalk mechanisms among channels, originated by some parasitic capacitances that couple individual channel operations. In particular, the strongest impact in crosstalk effects is introduced by the parasitic capacitance present between input and output amplifier terminals. This capacitance causes some charge variation at the instants when the integrating capacitors (i.e., capacitors B and D in Fig. 7) of any channel are connected in feedback to their respective amplifier. In fact, the stored charge must be shared with the parasitic capacitance, thus affecting the amplifier output voltage. To minimize these parasitic couplings, special care was taken when doing the layout of

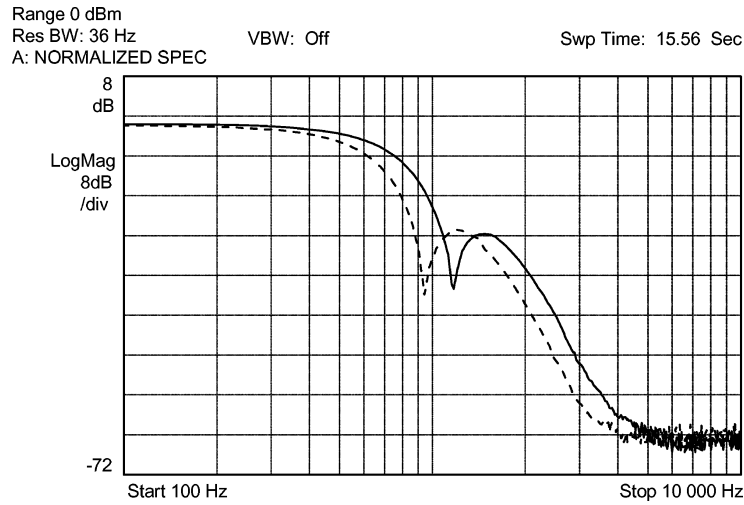
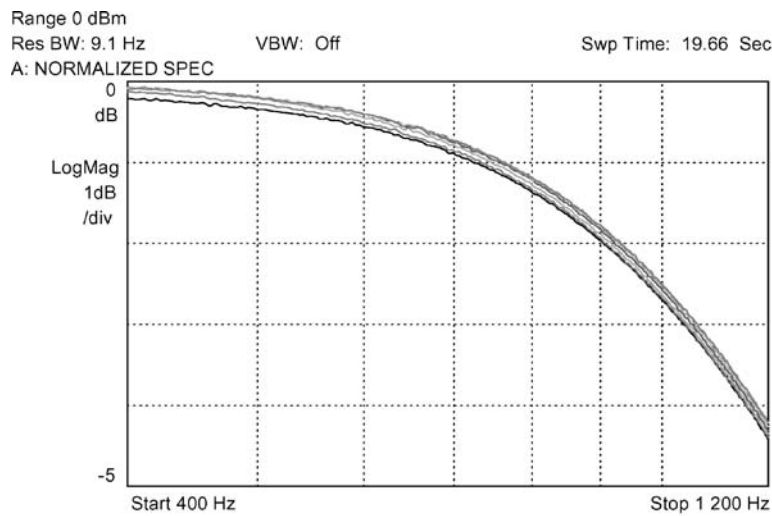
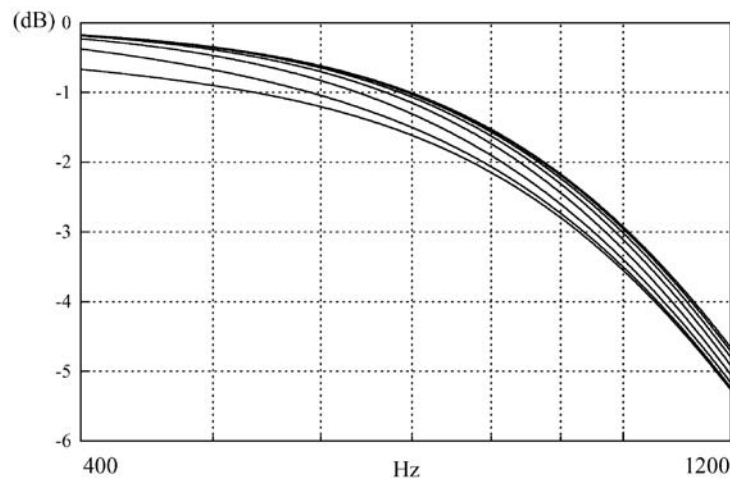


Fig. 10. Experimental response of the biquad section operating in series TM mode ($N = 4$) as a LP filter for the lower band in a speech inversion scrambler circuit: $f_{oi} = 1005$ Hz ($p_{f,eq,i} = 3.21875$, dashed line) and $f_{oi} = 1200$ Hz ($p_{f,eq,i} = 3.84375$, solid line).



(a)



(b)

Fig. 11. Crosstalk errors in f_o programmability for the LP response (circuit in Fig. 7 operating in TM parallel mode): (a) measured and (b) simulated.

the TM SC circuit. However, some unavoidable parasitic coupling exists due to the presence of feedback capacitors in the inactive channels. To evaluate the above crosstalk mechanisms, the equivalent capacitance C_{eq} of a single inactive amplifier feedback path in our filter was determined by simulations, obtaining a value around 35 fF.

The impact of crosstalk effects on f_{oi} programmability was then measured. To this end, the TM SC circuit was programmed to operate in parallel mode with $N = 2$, $m_1 = m_2 = 8$, selecting the LP response for both channels. Crosstalk measurements were carried out by setting the cutoff frequency f_{o1} of the first channel to 1 kHz ($p_{f,eq,1} = 1.625$), and sweeping the value of $p_{f,eq,2}$ in the second channel over the range $1.5 \leq p_{f,eq,2} \leq 1.71875$. Figure 11(a) shows the measured crosstalk-induced variations in the cutoff frequency of the first channel. Small crosstalk effects in the cutoff frequency can be observed. The TM SC circuit was also simulated by using SWITCAP with the same operating conditions as for the above measurements. The parasitic capacitance $C_{eq} = 35$ fF represented by any inactive channel was included. Shown in Fig. 11(b) are the simulated crosstalk errors, which agree very well with the experimental results.

Finally, Table 2 summarizes some measured parameters of the SC filter ($N = 4$) operating in series TM mode. THD measurements were carried out in the LP configuration with $f_{oi} = 2$ kHz ($p_{f,eq,i} = 6.40625$) using an input frequency f_{in} of 200 Hz. Negligible (i.e., within ± 1 dB) variations of THD were observed when varying the value of f_{oi} over a wide programmability range ($4 \leq p_{f,eq,i} \leq 6.40625$), while keeping the ratio f_{in}/f_{oi} constant so as to compare the results in a reliable way. The output noise power spectral density (PSD) was measured in all programmed LP responses, showing a roughly constant value of $1.3 \mu\text{V}/\sqrt{\text{Hz}}$ from dc up to 15.625 kHz. Both results demonstrate that the f_{oi}

Table 2. Measured performance of the SC filter operating in series TM mode ($N = 4$; Sampling frequency = 1 MHz).

Technology	CMOS 1.2 μm
Supply voltage	3 V
Programmability	8 bits: 3 integer–5 fractional
Power consumption	5.1 mW
THD (LP filter, $f_{oi} = 2$ kHz) ($V_{in} = 1 V_{pp}$ @ 200 Hz)	0.25%
THD (LP filter, $f_{oi} = 2$ kHz) ($V_{in} = 2 V_{pp}$ @ 200 Hz)	0.42%
IM3 (BP filter, $f_{oi} = 1.25$ kHz) ($V_{out} = 1 V_{pp}$ @ $f_{oi} \pm 10$ Hz)	0.6%
IM3 (BP filter, $f_{oi} = 1.25$ kHz) ($V_{out} = 1.5 V_{pp}$ @ $f_{oi} \pm 10$ Hz)	0.8%

programmability according to the proposed technique maintains the circuit dynamic range substantially constant. The third-order intermodulation distortion (IM3) was characterized over the BP response. The central frequency was set to $f_{oi} = 1.25$ kHz ($p_{f,eq,i} = 4$), and the test frequencies were $f_{oi} \pm 10$ Hz.

5. Conclusion

The operation of series/parallel time-multiplexed SC circuits programmable by a sort of non-uniform clock signals with noise-shaped sampling energy has been proposed. The programmability is realized from the digital domain, by means of a simple programmable logic section. It has been shown that very wide programmability range and high accuracy are obtained, with substantially no impact on the achievable dynamic range. Moreover, all the required clock signals are derived from a single master clock, which avoids the practical drawbacks associated with multiple-clock operation. The proposed technique allows the design and implementation of many digitally programmable analog functions. Experimental results obtained from an integrated test-chip demonstrate the versatility and potentiality for low-frequency applications.

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