

# Quasi Rail-to-Rail Very Low-Voltage OPAMP With a Single pMOS Input Differential Pair

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**Abstract**—In this brief, a quasi-rail-to-rail low-voltage operational amplifier ( $V_{DD} - V_{SS} - V_{DSATP} - V_{DSATN}$ ) is introduced. A common-mode adapter that uses the common-mode voltage present at the common-source node of the available differential pair to accommodate the large common-mode input signal is proposed. The common-mode adapter operates properly at 300 kHz while driving a load capacitor of 15 pF and employs only 95  $\mu$ W of static power. The amplifier was fabricated in a standard AMI 0.5- $\mu$ m CMOS process ( $V_{tn} = 0.7$  V and  $V_{tp} = -0.9$  V) and achieves an IM3 of  $-48$  dB at 300 kHz for a two-tone input signal of  $0.8 V_{pk-pk}$ . A 1-V total supply voltage was used.

**Index Terms**—Common-mode adapters, common-mode circuits, low-voltage amplifiers, low-voltage circuits, rail-to-rail amplifiers.

## I. INTRODUCTION

MODERN VLSI circuits require lower power consumption and the use of lower supply voltages, e.g.,  $\pm 0.5$  V. The use of low-voltage circuits with an input common-mode range that goes to both positive and negative supply rails is needed to fully exploit the available voltage room, especially for buffer and sample and hold applications [1]. One of the most important building blocks in analog and mixed-mode circuits is the OPERATIONAL AMPLIFIER (OPAMP). OPAMPs based on pMOS input differential pairs have good negative input common-mode range but limited positive common-mode range due to the voltage headroom needed for the operation of the amplifier's input stage. Similarly, nMOS differential pairs have limited negative common-mode range.

Several techniques to achieve rail-to-rail operation employ parallel n-channel and p-channel differential pairs to achieve rail-to-rail common-mode operation [2], [3]. A drawback of this approach is that for input voltages with a common-mode voltage in the middle voltage range, both differential pairs will be off, and only one differential pair is active when large signals are present. Therefore, it is difficult to match the transconductance of the two differential pairs. Other less popular approaches require depletion-mode transistors [4], floating voltage-controlled current sources [5], or higher voltage supply sources [6], [7]. Recently proposed strategies use a common-mode adapter that accommodates the input signal within the common-mode range of the input differential pair [8], [9]. In [8], a common-mode signal adapter makes use of two pseudodifferential pairs that

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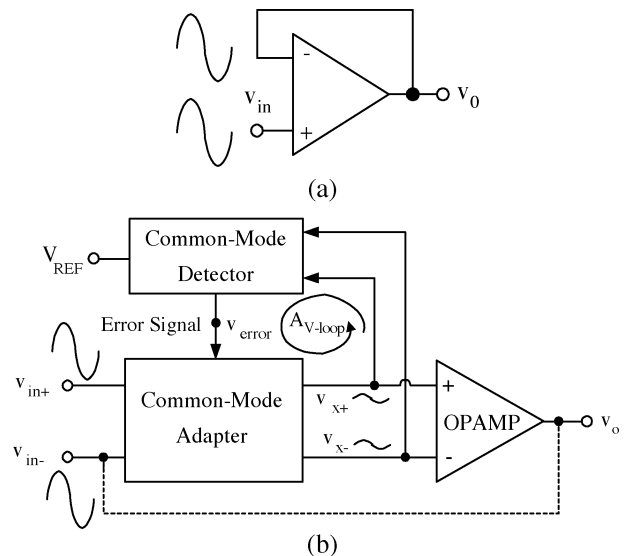


Fig. 1. (a) OPAMP in unity gain configuration. (b) Main concept behind the rail-to-rail amplifier.

increase circuit complexity and power consumption; this structure is discussed in the next section. The circuit reported in [9] adapts the common-mode input voltage by means of a feedback loop that controls a couple of floating gates operating as a capacitive voltage divider in front of the OPAMP, increasing the circuit area. Reliability of floating capacitors used and sensitivity to charge injection effects are other drawbacks in that topology.

In this brief, two of the aforementioned techniques are combined for the design of a quasi-rail-to-rail amplifier. The operation of the topologies reported in [8] and [9] is revised in Section II. The proposed amplifier is described in Section III. The experimental results that verify the effectiveness of the proposed techniques are presented in Section IV. The conclusions are provided in Section V.

## II. COMMON-MODE AMPLIFIER: PRINCIPLE OF OPERATION

As depicted in Fig. 1(a), a unity gain configuration requires an amplifier with a common-mode input range similar to the incoming signal while the differential signal at the OPAMP ( $= v_o/A_v$ ) input is very small. For an open-loop gain of 30 dB and  $v_o = 1 V_{pk-pk}$ , the differential signal at the input of the OPAMP is no more than 30 mV<sub>pk-pk</sub>. However, it is difficult to apply large swing input signals directly to the OPAMP mainly due to the limited common-mode range of its input stage. The common-mode input signal has to be further attenuated with the help of additional circuits before it is applied to the OPAMP; the concept is depicted in Fig. 1(b). It is worth mentioning that

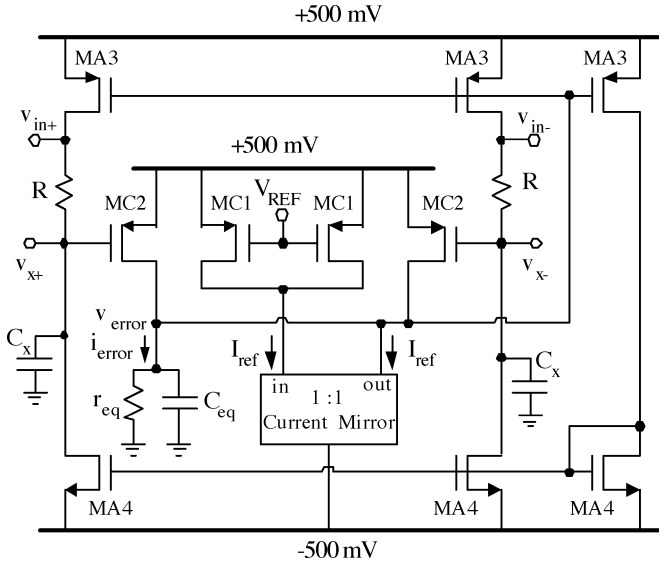


Fig. 2. Simplified schematic of the common-mode detector adapter reported in [8].

the common-mode adapter must operate on the common-mode signals only.

The common-mode adapter detects the common-mode voltage of the incoming signal, reduces it, and adjusts its dc level to be close to a reference voltage through a common-mode feedback loop. The differential behavior of the circuit is, in principle, not affected. The topology reported in [8] uses a single pMOS input differential pair for the OPAMP with a 1-V voltage supply.  $v_{in+}$  and  $v_{in-}$  are the inputs of the common-mode adapter while the differential signal  $v_{x+} - v_{x-}$  drives the OPAMP input stage; if the common-mode loop gain is high enough, the common-mode level of the OPAMP input signal  $v_{x-cm} = 0.5(v_{x+} + v_{x-})$  is forced to be close to the reference voltage  $V_{REF}$ .

The common-mode detector and the common-mode adapter operate similarly to the common-mode feedback loop used in fully differential circuits. Due to the action of the loop, the common-mode signal at the OPAMP input  $v_{x-cm}$  is given by

$$v_{x-cm} \cong \frac{v_{in-cm}}{(1 + A_{V\_loop})} + \frac{A_{V\_loop} V_{REF}}{(1 + A_{V\_loop})} \quad (1)$$

where  $A_{V\_loop}$  is the open-loop gain for common-mode signals, and  $v_{in-cm} = 0.5(v_{in+} + v_{in-})$ . Notice in (1) that the larger the loop gain is, the smaller the common-mode variations at nodes  $v_{x+,-}$  are; therefore,  $v_{x-cm}$  stays very close to  $V_{REF}$ . A simplified schematic of the common-mode adapter reported in [8] is depicted in Fig. 2.

The common-mode detector is implemented by transistors MC1 and MC2 and the current mirror. Due to the limited supply voltage, the implementation of the 1:1 current mirror is carried out by using cascode p-type current mirrors (not shown in Fig. 2, but details can be found in [8]). The reference voltage  $V_{REF}$  is set in the range of  $-400$  mV and is generated by using a replica of MC1; for zero input ( $v_{in+} = v_{in-} = 0$ ), the overall current consumption of the common-mode adapter is around  $213 \mu\text{A}$ .

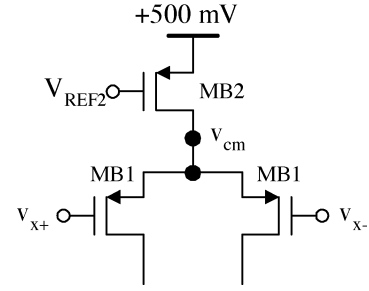


Fig. 3. Common-mode voltage detector [9], [10].

By using conventional circuit analysis techniques, it can be found that the common-mode adapter's open-loop gain has three poles, yielding

$$A_{V\_loop} \cong \frac{g_{mC2} g_{mA3} r_{eq} R}{(1 + s r_{eq} C_{eq})(1 + s R C_x) \left(1 + s \frac{3 C_{gsA4}}{g_{mA4}}\right)} \quad (2)$$

where  $r_{eq}$  and  $C_{eq}$  are the ac equivalent resistance and equivalent capacitor, respectively, at node  $v_{error}$ . The loop gain has two important poles located at  $\omega_{p1} = 1/r_{eq} C_{eq}$  and  $\omega_{p2} = 1/R C_x$ . Loop stability is guaranteed if the most important non-dominant pole, located at  $\omega_{p2}$  due to the relatively small resistance  $R$ , is placed beyond the unity gain frequency of the loop  $\omega_u = g_{mC2} g_{mA3} R / C_{eq}$ ; then, the loop gain must be designed such that

$$\frac{1}{R C_x} > \frac{g_{mC2} g_{mA3} R}{C_{eq}}. \quad (3a)$$

This stability condition can also be expressed as

$$R < \sqrt{\left(\frac{1}{g_{mA3} g_{mC2}}\right) \left(\frac{C_{eq}}{C_x}\right)}. \quad (3b)$$

Thus,  $R$  is limited to satisfy this condition; since  $R$  is located at the OPAMP input, its value is upper limited by noise considerations. In [9], an adaptive level shifter based on floating gate capacitors is used. The common-mode voltage is directly obtained from the common-source voltage of the p-type differential pair; a similar approach has been used for the common-mode detection of switched capacitor circuits as well [10]. The main concept is shown in Fig. 3. The common-source voltage is approximately given by

$$v_{cm} = v_{x-cm} + V_{SG} \quad (4)$$

where  $v_{x-cm}$  is the common-mode component of  $v_{x+}$  and  $v_{x-}$ . In [9], an auxiliary amplifier compares  $v_{cm}$  with a reference voltage, and the result is used to control the multiple input floating gate transistors that adjust the common-mode level. The common-mode loop gain is attenuated by a capacitive voltage divider that results in loop gain reduction and higher capacitive input impedance. The topology uses 3-V supply voltages and is not suitable for very low voltage applications.

### III. PROPOSED QUASI-RAIL-TO-RAIL AMPLIFIER

The proposed common-mode adapter is an extension of the aforementioned techniques; the concept is depicted in Fig. 4. The OPAMP used is composed of a single-ended folded cascode



TABLE I  
COMPONENT VALUES

Transistor	W( $\mu\text{m}$ ) / L( $\mu\text{m}$ )	$I_{\text{BIAS}}$ ( $\mu\text{A}$ )
Common-mode adapter (fig. 5)		
MA1	12/0.6	1.5
MA2	130/0.6	4.5
MA3	820/0.6	29
MA4	270/0.6	29
OPAMP (fig. 4)		
MB1	1000/0.6	10
MB2	240/0.6	20
MB3	120/0.6	10
MB4	40/0.6	10
MB5	90/0.6	20
MB6	730/0.6	50
MB7	260/0.6	50

TABLE II  
SUMMARY OF SIMULATION PERFORMANCES

Parameter	Reference [ 8 ]	This work
Adapter Power @ $v_{\text{in}}=0\text{V}$	213 $\mu\text{W}$	95 $\mu\text{W}$
DC Gain	60 dB	60 dB
GBW	3.74 MHz	4.13 MHz
Phase Margin	80°	83°
SR+, 0.9 V <sub>step</sub>	1.25 V/ $\mu\text{s}$	0.86 V/ $\mu\text{s}$
SR-, 0.9 V <sub>step</sub>	0.81 V/ $\mu\text{s}$	0.8 V/ $\mu\text{s}$
IM3 @ 0.8 V <sub>pk-pk</sub> , 100KHz	48 dB	50 dB

Under the most positive signal swing, the input voltage  $v_{\text{in}+}$  can be as large as 450 mV, while  $v_{x+}$  and  $v_{x-}$  remain around  $-400$  mV, leading to a maximum drain current in MA3 and MA4 of 55  $\mu\text{A}$  per branch. Therefore, the adapter peak current is around 165  $\mu\text{A}$ . The adapter's input resistance is in the order of 0.5  $\text{M}\Omega$  and is dominated by the parallel output resistance of transistors MA3 and MA4.

#### IV. SIMULATED AND EXPERIMENTAL RESULTS

The current-mode adapters shown in Figs. 2 and 5 were simulated using the design kit of the AMI 0.5-  $\mu\text{m}$  CMOS technology. The threshold voltages are in the range of 0.7 and  $-0.9$  V for the n- and p-type transistors, respectively. The supply voltages  $V_{\text{DD}}$  and  $V_{\text{SS}}$  are  $\pm 0.5$  V. A load capacitance  $C_L = 15$  pF was used. The OPAMP dc gain was in the range of 60 dB, and the third intermodulation distortion (IM3) is smaller than  $-50$  dB for a two-tone input signal of 0.8 V<sub>pk-pk</sub>. A comparison between the topology reported in [8] and the one reported here is presented in Table II. The proposed topology gives similar results to the existing solution while allowing a reduction in the dc power consumption by more than 50%.

The circuits were fabricated through the Mosis educational service; the chip microphotograph is shown in Fig. 6. The proposed amplifier's active area is 0.15  $\text{mm}^2$ , while the topology reported in [8] employs 0.22  $\text{mm}^2$ . The open-loop magnitude response of the proposed topology is shown in Fig. 7; the measured dc gain is around 41 dB. Compared with the expected 60 dB, there is a difference of 19 dB that is attributed to the external resistor (1  $\text{M}\Omega$ ) used for the amplifier's dc stabilization, the 1-  $\text{M}\Omega$  resistance of the active testing probe employed

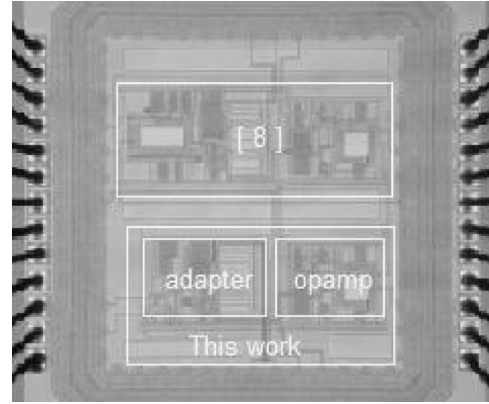


Fig. 6. Micrograph of the chip.

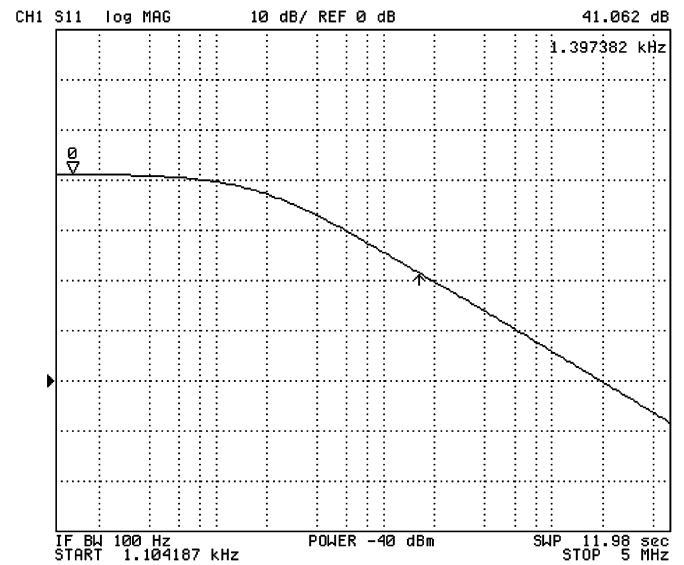


Fig. 7. Magnitude response of the proposed amplifier.

for chip characterization, and the lack of accuracy of the models when the transistors operate in the subthreshold region.

The measured unity gain frequency is around 2 MHz, which is smaller than the expected one. This difference is a result of the extra parasitic capacitors due to the testing board and the 8 pF lumped to the test equipment. The measured phase margin is better than 80°. No poles or zeros were observed at low frequencies, showing that the frequency response of the common-mode adapter was good enough such that the differential performance was not affected.

The linearity of the circuit was tested by using two-tone signals and observing the intermodulation distortions; for the following results, the circuit was tested in a closed-loop unity gain configuration. In Fig. 8, the IM3 results are shown; two tones with amplitude of 400 mV<sub>pk-pk</sub> each were applied. IM3 is around  $-50.8$  dB, which fits very well with the simulation results. The amplifier is able to operate up to 300 kHz, while IM3 is better than  $-40$  dB for signals of 800 mV<sub>pk-pk</sub>. A comparison between the experimental IM3 for the proposed structure and the one reported in [8] is shown in Fig. 9. The harmonic distortion of both topologies is within a difference of 3 dB up to 300 MHz. For the proposed architecture, the measured output

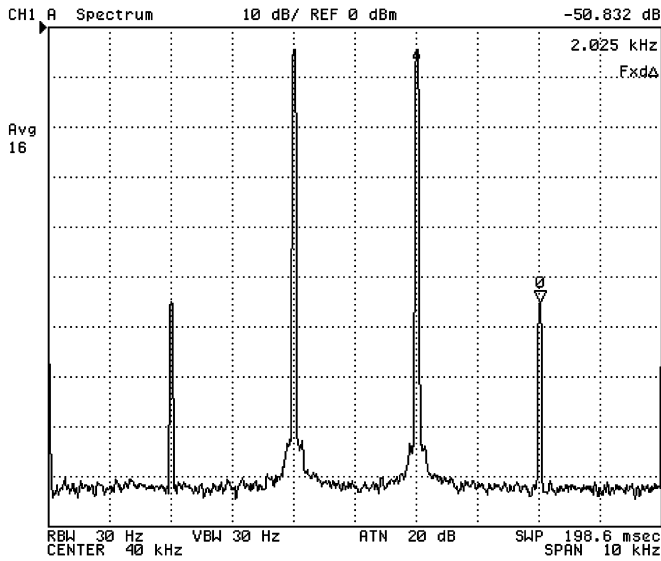


Fig. 8. IM3 measured at 40 kHz for two-tone signal of 800 mV<sub>pk-pk</sub>.

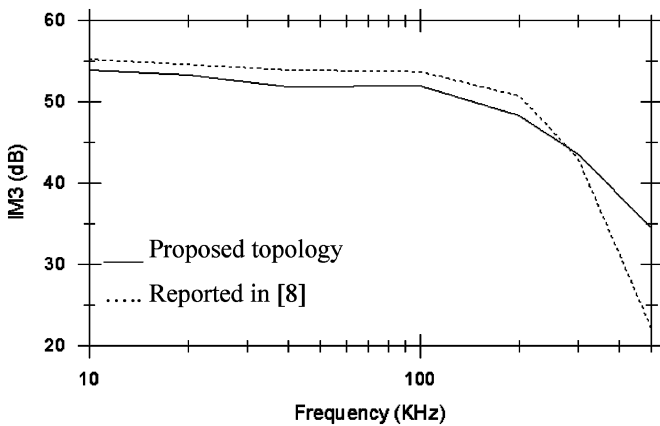


Fig. 9. IM3 measured results for various two-tone (400 mV<sub>pk-pk</sub> each) input frequencies.

noise density is in the range of  $-112 \text{ nV/Hz}^{1/2}$  at 100 kHz; low-frequency noise is dominated by flicker components, with a corner frequency of around 50 kHz. Table III presents a comparison of the experimental performance between the two topologies.

TABLE III  
SUMMARY OF EXPERIMENTAL RESULTS

Parameter	[8]	This Work
DC Gain	43.13 dB	41.04 dB
Phase Margin	74°	80°
IM3 @ 0.8 V <sub>pk-pk</sub> , 100 KHz	-53 dB	-50 dB
PSRR+	-61 dB	-57 dB
PSRR-	-49 dB	-48 dB
Noise Density at 100 kHz	130 nV/Hz <sup>1/2</sup>	112 nV/Hz <sup>1/2</sup>

## V. CONCLUSION

A low-voltage low-power common-mode adapter topology for rail-to-rail operation has been presented. The common-mode adapter is combined with a folded cascode OPAMP to operate with supply voltages of  $\pm 0.5 \text{ V}$ . To reduce circuitry and save power, this topology eliminates the use of extra common-mode detectors but still yields similar results compared with existing topologies. Experimental results show that the power consumption of the common-mode adapter can be reduced by more than 50%.

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