

On-Chip Testing Techniques for RF Wireless Transceivers

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This article describes a set of on-chip testing techniques and their application to integrated wireless RF transceivers. The objective is to reduce final product cost and accelerate time to market by providing means of testing the entire transceiver system as well as its major building blocks without using off-chip analog or RF instrumentation. On-chip test devices fabricated in a standard CMOS process and experimentally evaluated support the proposed test strategy.

robustness, transparency to DUT operation, and low area overhead. This article proposes the application of recent BIST techniques and a loop-back architecture as a strategy to improve a wireless transceiver's testability. Our objective is to enable measurement of the major performance metrics of the transceiver and

■ **WIRELESS COMMUNICATION DEVICES**, among the semiconductor industry's most important products, are gathering a continually growing number of standards and applications. In today's competitive market, incorporating a comprehensive testing strategy into a wireless module's design flow is indispensable to its timely development and economic success.¹⁻³ Modern transceivers are highly integrated systems. Their diverse specifications and components and high frequencies of operation make testing them complex and expensive. Increasing the effectiveness and cost efficiency of analog and RF tests in integrated systems is a complex problem that researchers have addressed at various levels. Recent efforts include defect modeling, automated test algorithms, alternate tests for system specifications,⁴ DFT techniques,^{5,6} and BIST techniques.⁷⁻¹¹

BIST, in particular, can become a high-impact resource for several reasons. First, to reduce the complexity and cost of external ATE and its interface to the device under test, it is desirable to move some testing functions to the test board and into the device under test (DUT) itself.^{2,3} Second, increasing packaging costs demand known-good-die testing solutions that can be implemented at wafer level.⁶ Third, BIST's fault location capabilities (that is, to identify a faulty block in the system) provide valuable feedback for yield enhancement, thus accelerating product development.

Nevertheless, to be effective in systems with RF and analog components, BIST must meet requirements of

its building blocks at wafer level, while avoiding the use of RF instrumentation. Figure 1 illustrates this approach. The embedded testing devices communicate with the ATE through an interface of digital signals and DC voltages. From the extracted information on the transceiver's performance at intermediate stages, the ATE not only detects but also locates catastrophic and parametric system faults.

Switched loop-back architecture

A loop-back connection between transmitter and receiver chains is one of the earliest strategies devised for testing wireless and wire-line communication system functionality.⁵ It doesn't require an external stimulus, and is effective at detecting catastrophic faults in the complete signal path. Figure 2a depicts this testing scheme for a transceiver architecture with direct up-conversion. In a complete realization, the baseband sections include in-phase (I) and quadrature (Q) paths, but this block diagram shows only one path for simplicity.

In the loop-back configuration, the transmitter's baseband section generates a tone or a modulated signal (M) with center frequency f_b . With input from the local oscillator (LO) at frequency f_{RF} , the up-converter generates a tone (U) at $f_b + f_{RF}$. The loop-back connection must attenuate the power amplifier (PA) output to make it suitable for the dynamic range of the low-noise amplifier (LNA). After down-conversion with the same LO tone, the resultant signal (D) at the receiver base-

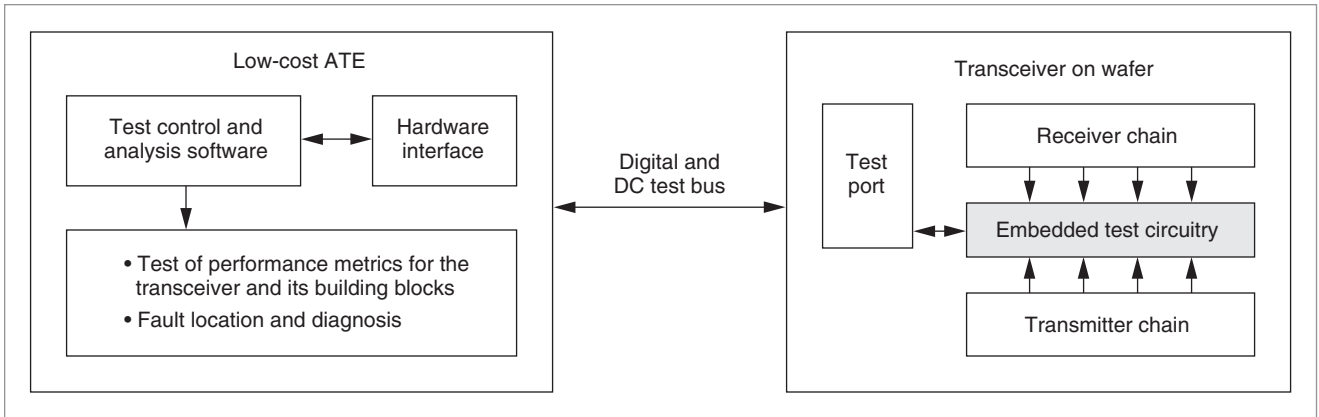


Figure 1. Objective of the proposed set of on-chip testing techniques: wafer-level transceiver testing with a low-cost ATE.

band is centered at f_b . The ATE can analyze the demodulated or digitized signal's characteristics to evaluate the transceiver's performance. In this configuration, the transmitter baseband limits the range of f_b values.

Recent radio implementations use transmitter architectures in which the transmitted signal is modulated directly on the voltage-controlled oscillator (VCO), avoiding up-conversion.^{12,13} As Figure 2b shows, direct application of loop-back test is not practical in this kind of transceiver. A DC decoupling mechanism is usually included at one or more points in the receiver's baseband section to prevent DC offsets from saturating the demodulator or ADC. Because the signal at the PA output has the same frequency as the one used for the down-conversion mixer, only a DC voltage will be obtained after the mixer and this information is lost. To overcome this limitation of loop-back test in a VCO-modulating transceiver, Ozev and Olgaard have proposed introducing a delay in the loop-back connection, as well as a digital DFT modification in the modulator.⁶ This strategy is a way to detect catastrophic faults and measure some of the transceiver's important performance metrics. However, the required delay is implemented off chip, requiring an RF signal flow outside the wafer and thus increasing setup cost and complexity.

Figure 2c illustrates the principle of operation of our proposed switched loop-back technique applied to a transceiver with direct VCO modulation. If the signal in the loop-back path is switched at frequency f_{sw} , two additional tones are created at frequencies $f_{RF} \pm f_{sw}$. After the mixing with f_{RF} in the receiver, both tones are down-converted to f_{sw} . Thus, the frequency of the signal that controls the switch determines the frequency of the signal at the baseband chain. Conceptually, this is

equivalent to introducing a mixer in the loop-back path, but a simple switch is a suitable frequency translation device in this application. An important practical consideration is that in the off state, the switch must connect the LNA input to a 50- Ω resistor and not directly to ground to preserve the LNA's stability.

We model the operation of the switch on the signal from the PA as a multiplication between the RF signal and a square wave from 0 to 1. We describe such a train of pulses in the time domain as

$$\begin{aligned}
 P(t) &= \sum_{n=0}^{\infty} K_n \cos(n\omega_{sw}t + \theta_n) \\
 &= K_0 + K_1 \cos(\omega_{sw}t + \theta_1) \\
 &\quad + K_2 \cos(2\omega_{sw}t + \theta_2) + \dots
 \end{aligned}$$

where $\omega_{sw} = 2\pi f_{sw}$, and K_n and θ_n are constants that define the amplitude and phase of each frequency component, respectively. The product of $P(t)$ and the RF signal with amplitude A and frequency f_{RF} results in switched signal $S(t)$:

$$\begin{aligned}
 S(t) &= \left[\sum_{n=0}^{\infty} K_n \cos(n\omega_{sw}t + \theta_n) \right] \cdot A \cos(\omega_{RF}t) \\
 &= \frac{A}{2} \left\{ \begin{aligned} &2K_0 \cos(\omega_{RF}t) + K_1 \cos[(\omega_{RF} - \omega_{sw})t + \theta_1] \\ &+ K_1 \cos[(\omega_{RF} + \omega_{sw})t + \theta_2] \\ &+ K_2 \cos[(\omega_{RF} + 3\omega_{sw})t + \theta_3] \\ &+ K_2 \cos[(\omega_{RF} - 3\omega_{sw})t + \theta_4] + \dots \end{aligned} \right\}
 \end{aligned}$$

where $\theta_1, \theta_2, \dots, \theta_n$ are the phases corresponding to each new frequency component.

Finally, after the second multiplication at the receiver's mixer, down-converted signal $D(t)$ becomes

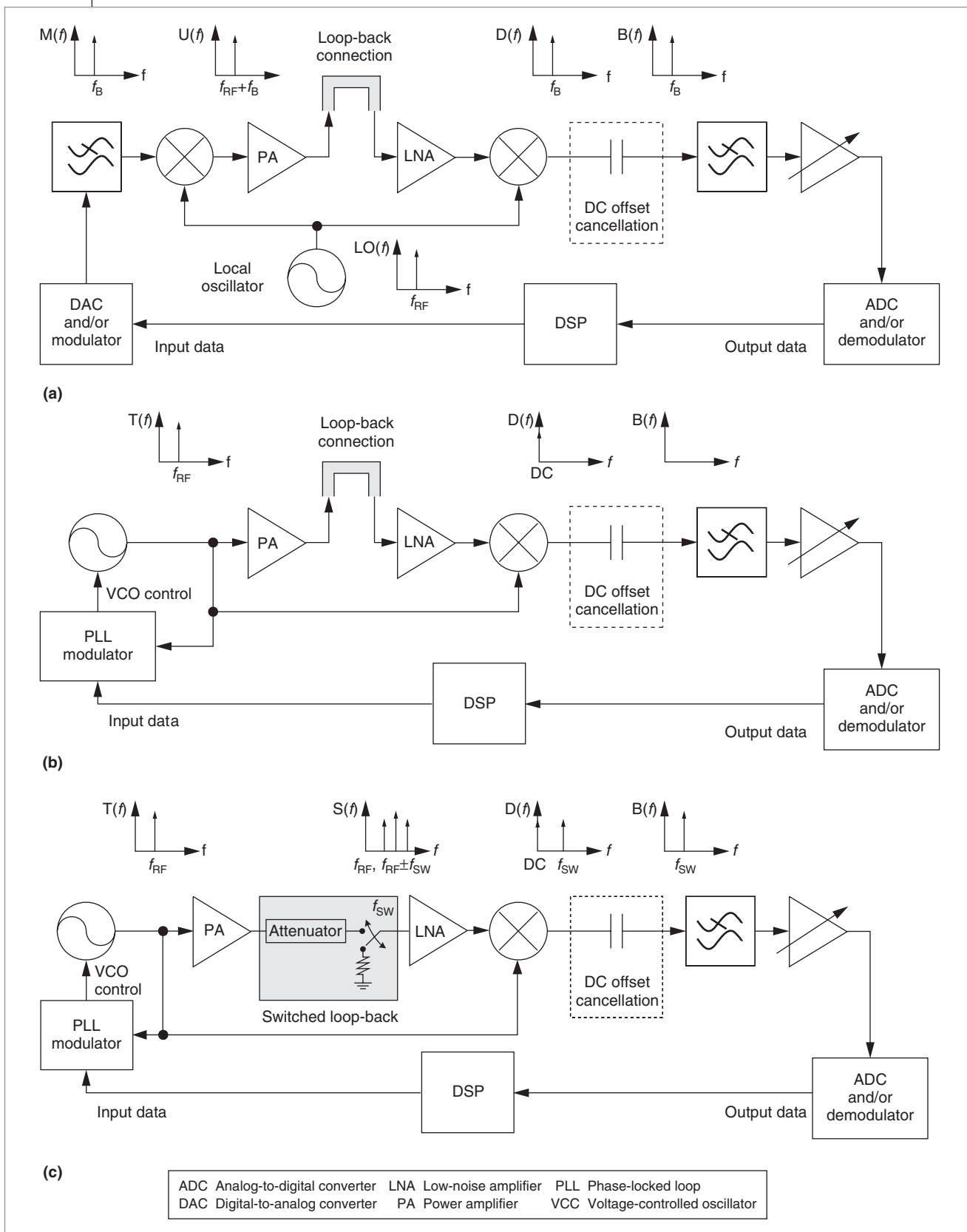


Figure 2. Loop-back architectures: standard technique in an up-conversion transmitter (a), standard technique in a direct VCO modulation transmitter (b), and proposed switched configuration (c).

$$\begin{aligned}
D(t) &= \left[\sum_{n=0}^{\infty} K_n \cos(n\omega_{sw}t + \theta_n) \right] \cdot A \cos(\omega_{RF}t) \\
&\quad \cdot B \cos(\omega_{RF}t + \alpha) \\
&= C_0 + C_1 \cos(\omega_{sw}t + \beta_1) + C_2 \cos(3\omega_{sw}t + \beta_2) \\
&\quad + C_3 \cos(5\omega_{sw}t + \beta_3) + \dots \\
&\quad + E_1 \cos\left[(2\omega_{RF} + \omega_{sw})t + \gamma_1\right] \\
&\quad + E_1 \cos\left[(2\omega_{RF} - \omega_{sw})t + \gamma_2\right] + \dots
\end{aligned}$$

where α , β_n , and γ_n are phase constants. The final amplitude of each frequency component (C_n , E_n) depends on the local oscillator's amplitude B , as well as on the mixer's conversion gain. The DC offset cancellation circuitry blocks DC component C_0 , and frequency components located around $2f_{RF}$ have negligible amplitude because a down-conversion mixer's output shows a low-pass characteristic. In addition, C_2 , C_3 , ... C_n depend on the nondominant frequency components of $S(t)$ and hence are small in comparison with C_1 .

One of this approach's most important advantages is that the loop-back connection can have a simple on-chip implementation. Switches and a bank of resistors or capacitors can implement a programmable attenuator, and a simple CMOS switch can commutate the signal at the LNA input. Yoon and Eisenstadt demonstrated an integrated implementation of this kind of switch.⁷ In the architecture proposed in this work, the switching signal is a digital clock with frequency f_{sw} in the MHz range, which can be easily applied to the transceiver on wafer. The ATE can directly control f_{sw} and thus can measure the transmitter and receiver chains' frequency responses independently.

Like the delayed loop-back test scheme, our switched loop-back architecture guarantees the continuous flow of a test stimulus throughout a wireless transceiver. However, it does not require an external RF component or modification of the modulator's implementation, thus achieving a test solution with lower implementation complexity and cost.

Analog and RF circuit testing

Limitations of a stand-alone loop-back test are that it cannot identify the location of catastrophic faults (such as an open in the signal path) and that some important parametric faults can pass undetected. For example, a higher gain in the PA or mixer can mask a lower gain in the LNA. Thus, a more effective testing strategy must incorporate means of verifying the receiver's operation at intermediate stages of the signal path, not only at its end points. A significant number of BIST techniques

have appeared in the literature, but most only with results from simulations or prototypes with discrete components, without addressing practical issues for integrated implementation. To this end, Valdes-Garcia et al. developed two different testing techniques and their associated devices and evaluated them with integrated prototypes.^{10,11} This work emphasizes circuit-level design to realize robust, very compact testing devices that impose an insignificant capacitive parasitic load and thus don't affect the DUT's operation.

The first of these techniques targets characterization of baseband blocks in the tens-to-hundreds MHz range. Figure 3a shows the principle of operation. At a given frequency ω_0 , an amplitude and phase detector (APD), based on an analog multiplier, observes the DUT's input and output signals and generates a vector of three DC voltages. From this vector, and by using simple arithmetic operations, the ATE computes the amplitude amplification/attenuation and phase shift introduced by the DUT. By performing this operation at different frequencies, the ATE can obtain a measurement of the DUT's frequency response over a bandwidth of interest. A significant advantage of this technique is that the performed measurements are insensitive to the test signal's amplitude, its harmonic distortion, and the analog multiplier's gain.¹⁰

A digitally programmable signal generator, a demultiplexer, and the APD form a complete frequency response characterization system (FRCS). The multiplexer allows the selection of two nodes from a set of multiple observation points. Thus, a single FRCS can extract the individual transfer function of each block in an integrated system such as a receiver's baseband chain. In experimental on-chip testing of continuous-time filters, the FRCS achieved an accuracy better than 1 dB for frequency response measurements of up to 130 MHz.¹⁰

The second technique is RF root-mean-square (rms) detection. Devices that generate a DC voltage proportional to RF power have proven effective for testing RF systems at board level.^{2,8} The use of embedded peak detectors for testing an integrated 5-GHz LNA has also been demonstrated in a SiGe BiCMOS implementation.⁹ However, current low-cost communication systems require CMOS solutions. Valdes-Garcia et al. have proposed a very compact CMOS RF rms detector (RFD) and a methodology for its use in on-chip characterization of the gain and 1-dB compression point of RF circuits.¹¹ Figure 3b depicts a conceptual description of this device's application. By placing a detector at the RF DUT's input and output, we can measure the device's gain at a given input power level regardless of the

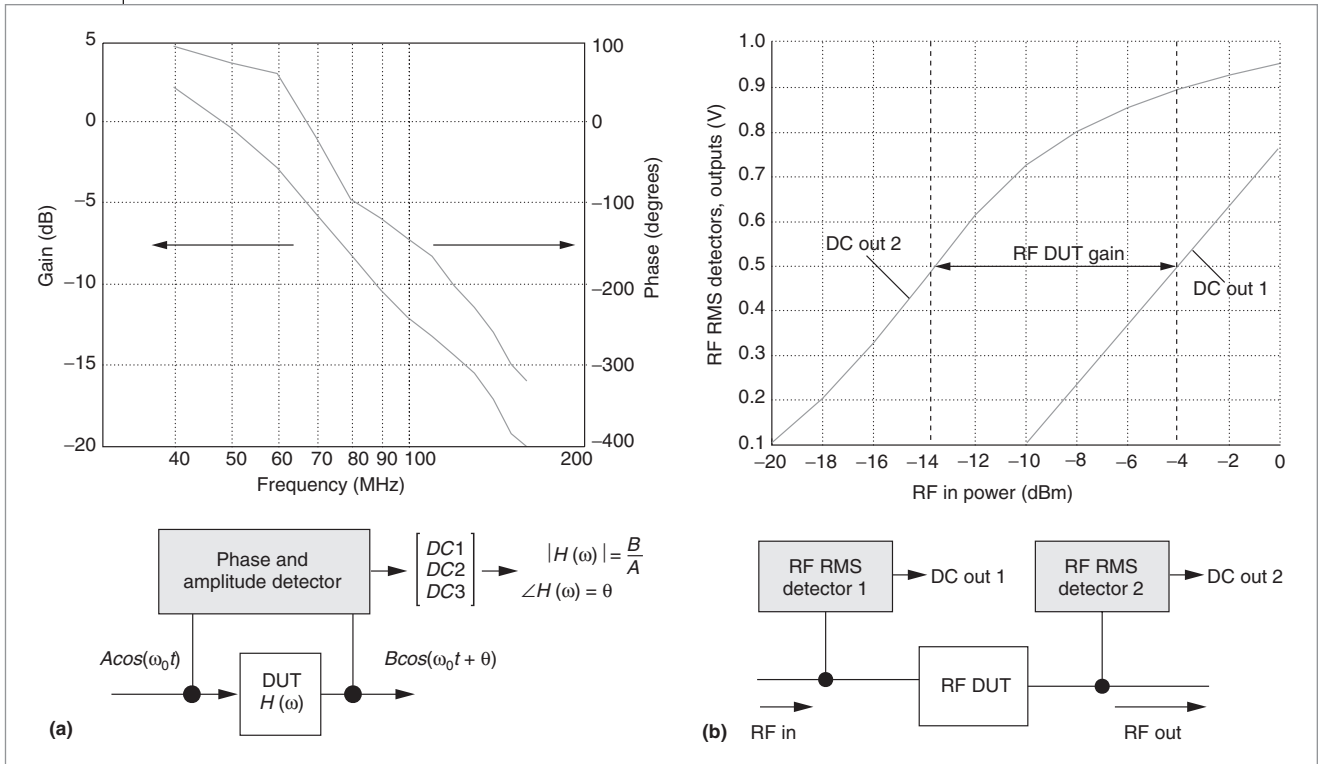


Figure 3. On-chip testing techniques: frequency response characterization (a); RF root-mean-square (rms) detection (b).

Table 1. Measured performance of on-chip testing devices.

Frequency response characterization system (FRCS)	
Operation frequency	DC-130 MHz
Amplitude detection dynamic range	> 30 dB
Phase detection resolution	< 1 degree
Input capacitance	50 fF
Settling time	< 400 ns
Power consumption	10 mW
Area	0.2 mm ²
RF RMS detector (RFD)	
Operation frequency	0.4-2.8 GHz
Linear dynamic range	20 dB
1 dB compression	Up to 10 dBm
Input capacitance	20 fF
Settling time (detection at 2.4 GHz)	< 40 ns
Power consumption	10 mW
Area	0.02 mm ²
DC-to-digital converter (DCDC)	
Resolution	7 bits
Conversion time	10 μs
Power consumption	100 μW
Area	0.1 mm ²

absolute value of the detector’s gain. This technique has achieved an accuracy of 1 dB in the measurement of gain and the 1 dB compression point in testing an integrated LNA operating at 1.7 GHz.

Because both the FRCS and the RFD have a DC output, an algorithmic DC-to-digital converter (DCDC) serves as a fully digital interface with the ATE. Circuit-level details of the RFD, the FRCS, and the DCDC are described in other publications.^{10,11} Table 1 shows a summary of experimental results from the IC prototypes fabricated in the standard TSMC 0.35-micron CMOS process through the MOSIS service.

Overall testing strategy

Joint application of the techniques just described can act synergistically to improve an entire integrated system’s testability. Figure 4 depicts a transceiver using a direct conversion transmitter with a switched loop-back connection, RFDs in the RF section, and an FRCS in the baseband section. The DCDC acts as an interface between the on-chip testing circuitry and a digital port of the ATE.

We can test the entire transceiver chain, except the transmitter’s baseband circuitry, by using the LO signal and the switched loop-back connection. A complete end-

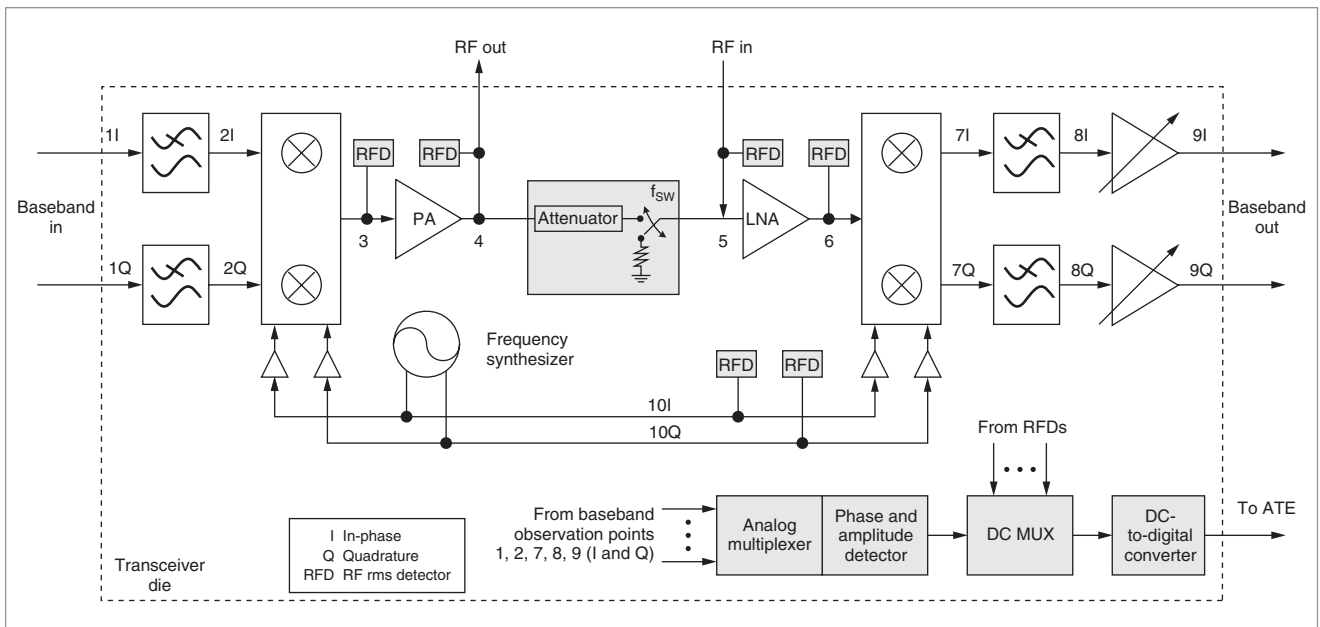


Figure 4. Integrated transceiver with improved testing capabilities.

Table 2. Transceiver testing methods with proposed architecture (Figure 4). (I and Q represent in-phase and quadrature paths.)

Test	Test device and method	Observation nodes
LNA gain and 1 dB compression point	RFDs—sweep input power to LNA by changing the transmitter output power or the loop-back attenuator loss	5, 6
PA gain and 1 dB compression point	RFDs—sweep input power to PA by varying the up-converter gain	3, 4
Up-converter operation and output power	RFD	3
Synthesizer operation and output power for I and Q branches	RFD	10 (I and Q)
Phase and magnitude mismatch between I and Q baseband channels	FRCS	7, 8, 9 (I and Q)
Transmitter-filter transfer function	FRCS—sweep input frequency to transmitter across desired characterization range	1, 2 (I and Q)
Channel-selection-filter transfer function	FRCS—sweep f_{sw} across desired characterization range	7, 8 (I and Q)
Adjacent channel rejection	FRCS—set f_{sw} at adjacent channel frequency	8 or 9
Baseband amplifier gain programmability	FRCS	8, 9 (I and Q)

to-end test requires application of a low-frequency signal at the transmitter’s input either from the ATE or from an on-chip signal generator such as the one proposed for the FRCS.¹⁰ The switched loop-back connection guarantees flow of a test stimulus throughout the transceiver path, which the embedded testing devices can use to evaluate performance metrics at intermediate points of the system.

By providing independent control of signal frequency across the transmitter and receiver chains and providing access to internal points in the RF and baseband sections, we improve the receiver’s testability. Table 2

describes the tests possible in the proposed architecture. A complete testing solution for a given transceiver might not require performing all the possible tests.

Figure 5 shows a hierarchical testing strategy for the proposed architecture. The first step is an end-to-end test using the switched loop-back connection without involving the internal test devices. In this test, the ATE analyzes the final output from the receiver chain. The test provides measurement results for the transceiver’s overall performance metrics (such as overall gain), and it can detect that a catastrophic fault is present in the

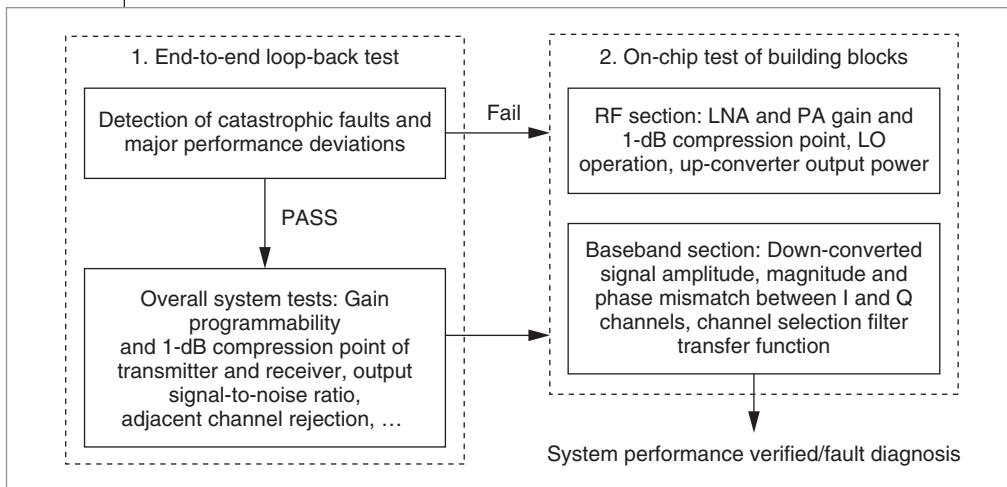


Figure 5. Flow diagram of proposed testing strategy.

Table 3. Area overhead analysis for reported transceivers.

Standard	Analog area (mm ²)	CMOS process (μs)	Overhead (%) of six RFDs, FRCS, and DCDC (0.45 mm ²)
Bluetooth ¹²	5.90	0.18	7.6
DECT ¹³	9.40	0.25	4.8
802.15.4 (ZigBee) ¹⁴	8.75	0.18	5.1

Table 4. Specifications of modeled ZigBee transceiver.

Specification	Description
RF frequency	2.4 GHz
Transmitter architecture	Direct conversion
Transmitter power	0 dBm
PA gain	15 dB
Receiver architecture	Low intermediate frequency (IF = 4 MHz)
Sensitivity	-82 dBm
RF front-end IIP3	-4 dBm
RF front end gain	30 dB (LNA 15 dB + mixer 15 dB)
Baseband filter	5th-order band-pass polyphase

system—for example, that no signal is present at the output or that the signal’s amplitude is far from the expected value. These system-level test results can help in selecting subsequent block-level tests—for example, to identify the cause of a specific faulty behavior. In the second step, the on-chip test circuitry locates a catastrophic fault and/or identifies parametric faults such as a deviation in baseband filter frequency response or a mismatch between I and Q signal paths.

We intend the proposed testable transceiver archi-

tecture to serve as a basis for a comprehensive testing strategy in which fault analysis, alternate system-level tests, and other techniques can optimize fault coverage and test efficiency. A complete test optimization procedure depends on the specific transceiver to be tested and is beyond the scope of this article.

As Table 1 shows, the settling time of the embedded test devices is on the order of nanoseconds. Therefore, the reading time of each of their DC outputs is dominated by the DCDC converter’s conversion time, which is 10 microseconds. This time will be significantly shorter for an implementation in current deep-submicron technologies or if the DC outputs are digitized in the ATE. The transceiver’s overall test time, for several hundreds of measurement points from the on-chip test devices, will be on the order of milliseconds. Moreover, because digital outputs from the test devices are closely related to system and building block specifications (gain, compression point, phase shift, and so forth), information processing overhead for the ATE is low.

Table 3 presents an analysis of area overhead that the added on-chip test circuitry represents with respect to the size of recently reported 2.4-GHz transceivers for various standards. Although the area shown for the testing devices is from prototypes in CMOS 0.35-micron technology, the area overhead is less than 10%.

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Simulation results

To analyze the proposed testing scheme’s performance, we built a macromodel of the transceiver architecture shown in Figure 4, including the switched loop-back connection and the RFDs, in the SystemVue simulation environment. The model’s components include the most important nonidealities expected from an integrated implementation, such as noise, signal compression, nonlinearity, and finite isolation between ter-

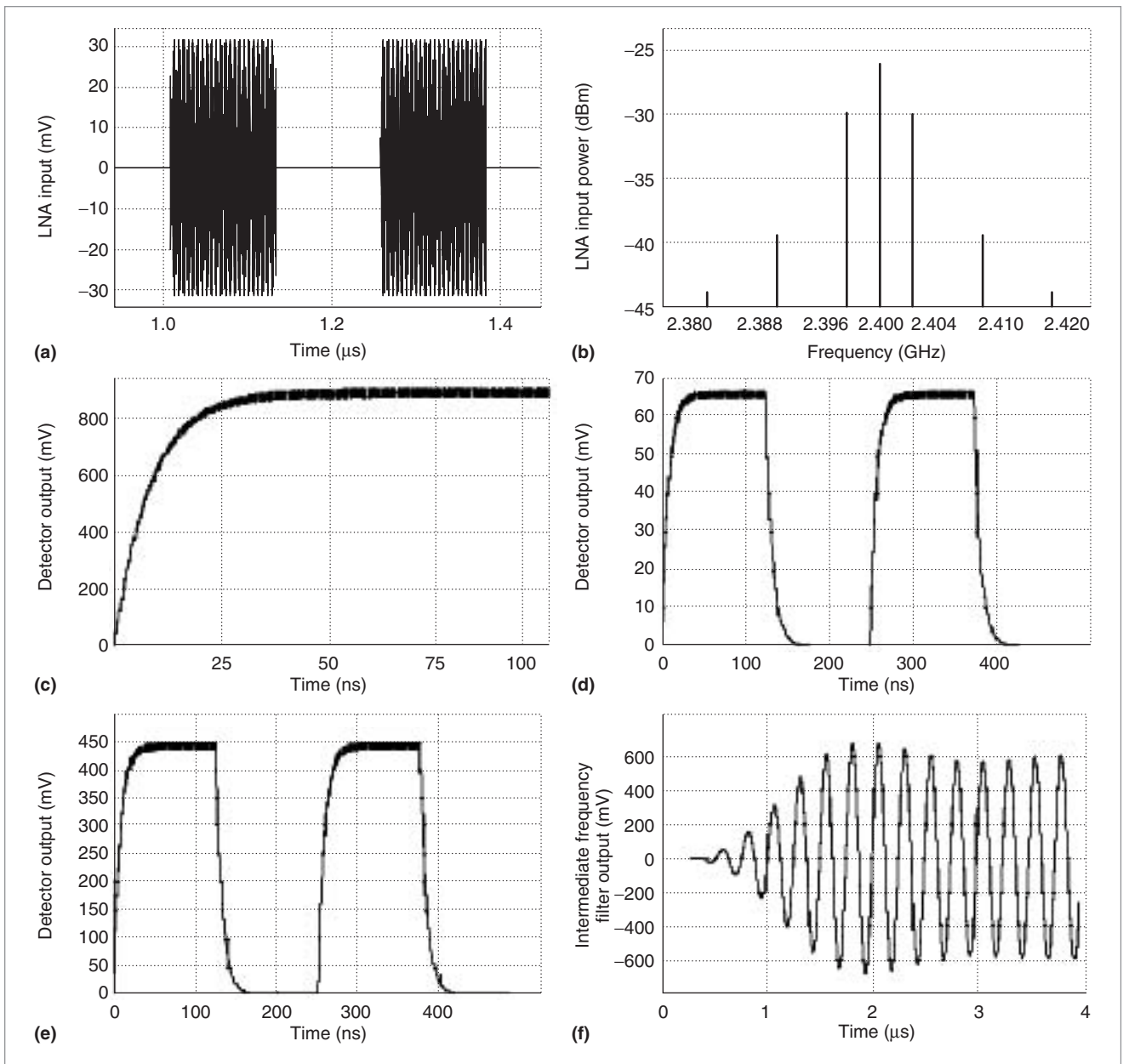


Figure 6. Simulation results for a transceiver meeting specifications: LNA input in time domain (a), LNA input in frequency domain (b), RFD output at PA output (c), RFD output at LNA input (d), RFD output at LNA output (e), and baseband filter output (f).

minals. Table 4 summarizes the modeled architecture's characteristics, which we took from the transceiver reported by Choi et al.¹⁴ We chose an IEEE 802.15.4 implementation because this standard targets very low cost applications. The attenuator in the loop-back connection has a 25-dB loss to bring the PA's 0-dBm output within the receiver's linear range. We modeled the RFDs according to the characteristics listed in Table 1.

Figure 6 shows simulation results for a transceiver

meeting specifications. The loop-back switching frequency is 4 MHz, because this is the baseband filter's center frequency. Figures 6a and 6b show the switched signal at the LNA input in the time and frequency domains. Observe that the frequency components of interest ($2,400 \pm 4$ MHz) are at least 10 dB above other tones. Figures 6c, 6d, and 6e show the outputs of the RFDs at the PA output, the LNA input, and the LNA output. Finally, Figure 6f shows the expected 4-MHz signal

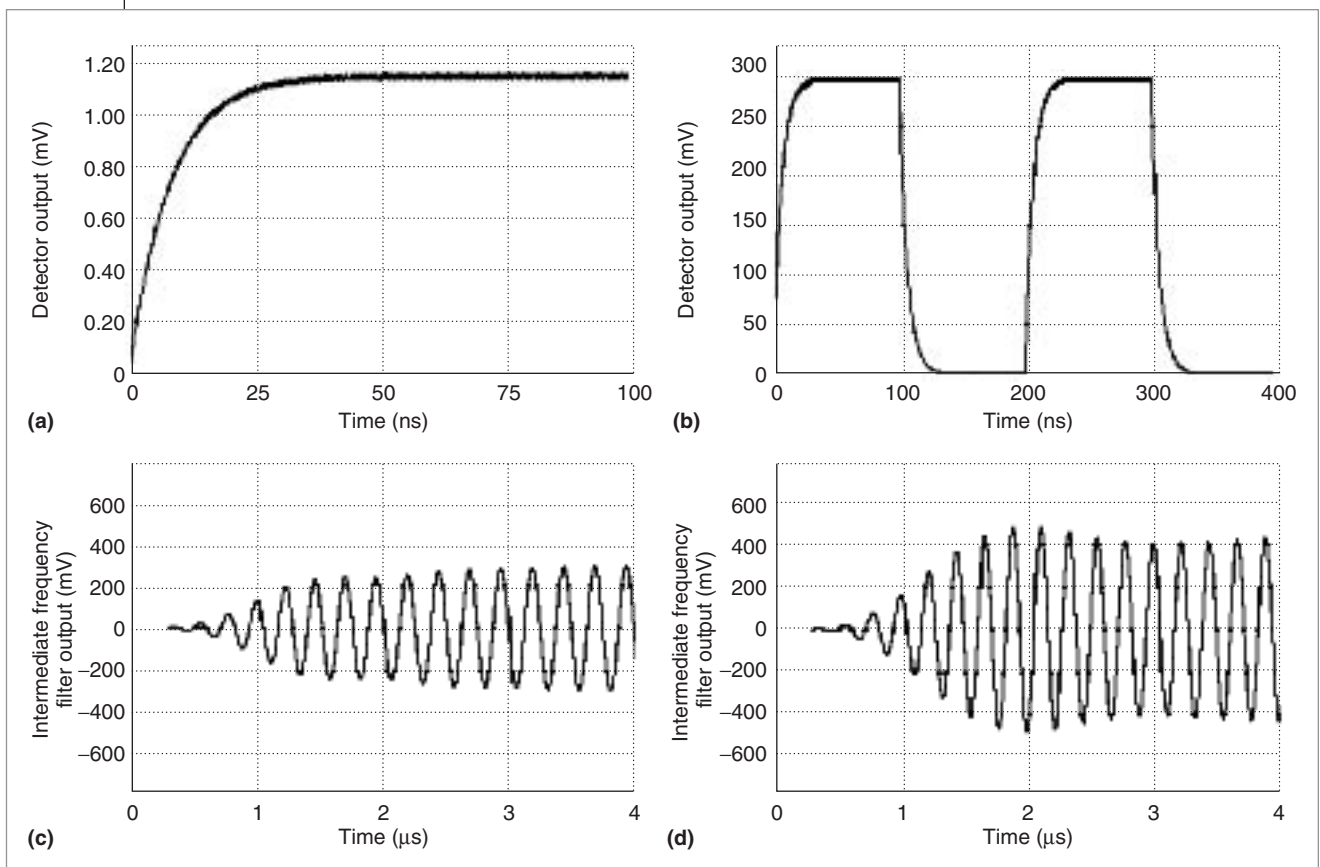


Figure 7. Simulation results for a transceiver not meeting specifications: output of the RFD at the PA output (a), output of the RFD at the LNA output (b), baseband filter output for $f_{sw} = 4$ MHz (c), and baseband filter output for $f_{sw} = 4.5$ MHz (d).

at the baseband filter's output.

Although the output of the RFDs placed after the switch is intermittent, we can still estimate the LNA gain, provided that the DCDC samples the RFDs' output at the appropriate rate. In the presented model, the DCDC has about 100 ns to sample each detector's output. In a scenario with a slower DCDC, we can first set f_{sw} to a lower value (so that the RFDs hold their output for a longer time) to test the LNA, and then shift to a higher value to test the rest of the receiver chain.

Figure 7 shows simulation results for a transceiver in which some of the individual building blocks do not meet target specifications. The PA has a 2-dB higher gain (12 dB total); the LNA has a 5-dB lower gain (10 dB total); and the channel selection filter is not centered at 4 MHz, but at 4.5 MHz. Figures 7a and 7b show the output of the RFDs at the PA and LNA outputs. Obviously, these final values are different from the ones shown in Figure 6. Figures 7c and 7d show the channel selection filter's output for $f_{sw} = 4$ MHz and $f_{sw} = 4.5$ MHz.

Note that a stand-alone end-to-end test could not determine the cause of a reduced amplitude at the end of the receiver baseband. Moreover, if both the PA and the LNA exhibited a higher gain, the receiver's output would show the expected amplitude even if the filter had a deviated center frequency. With a conventional loop-back test without the switch, changing the frequency of the input signal to the transmitter would enable us to determine that the fault is occurring at the baseband but not whether it is on the transmitter or receiver side. With the proposed scheme, we can detect and locate parametric faults in different sections of the system.

ADDRESSING FUNDAMENTAL circuit-level issues of a test strategy yields an efficient and feasible solution. Extending the proposed concepts to implementations in current deep-submicron technologies opens significant opportunities for improved performance as well as the solution to new challenges. ■

Acknowledgments

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