

Multipath common-mode feedback scheme suitable for high-frequency two-stage amplifiers

A.K. Gupta, V. Dhanasekaran, K. Soundarapandian and E. Sanchez-Sinencio

A method for stabilising the common-mode feedback (CMFB) loop in high-speed fully differential two-stage amplifiers is presented. Existing approaches may prove to be inadequate for high-speed designs. The problem becomes acute because of positive DC feedback by external network, which leads to 'latching states'. The proposed multipath approach avoids the latching states while maintaining the stability of the CMFB loop.

Introduction: Fully differential amplifiers are widely used in modern integrated circuits because of larger output swings and less susceptibility to common-mode (CM) noise. One major disadvantage of these circuits is the need of a CMFB circuit to control the CM output voltage. The basic aim of the CMFB circuit is to sense the output CM voltage and use negative feedback to force it equal to the desired CM voltage V_{REF} . In this Letter, we analyse a case of practical interest in which the negative feedback loop is no longer effective because of positive feedback by the external network, leading to the output staying at the rails [1]. The existing solutions [2] will need a large bandwidth in the CMFB loop to alleviate the situation, making it difficult to compensate for high-speed designs. The proposed scheme tackles the problem by having large transconductance gain at low frequencies while having a low transconductance gain at high frequencies in the CMFB loop.

External positive feedback and latching states: One of the various methods to detect and feedback the CM correction signal as applicable to a two-stage amplifier is shown in Fig. 1. Only a fraction ($I_3/(I_3 + I_4)$) of the total current is controlled by the CM loop. The DC error in the CM output is given by

$$\Delta V_{OCM} = V_{REF} - V_{OCM} = \frac{\Delta I}{g_{m3}A_1} \quad (1)$$

where ΔI is the open-loop mismatch between the current sources ($I_{1o} + I_{2o} - I_{3o} - I_{4o}$) and A_1 is the voltage gain of the CM sense amplifier shown in broken lines in Fig. 1. Thus we observe that the error will reduce if we increase the transconductance gain ($g_{m3}A_1$).

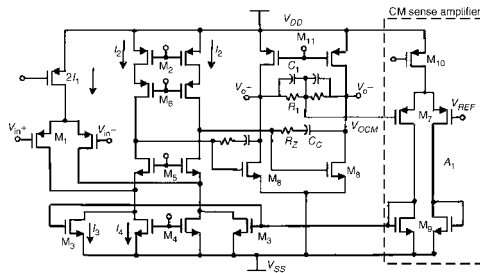


Fig. 1 Two-stage Miller compensated amplifier with traditional resistor averaged CMFB scheme

For a two-stage amplifier, although the feedback through the external network is negative for the differential signal, it is positive for the CM signals. In normal operating conditions, the negative feedback loop gain is much larger compared to the positive feedback loop gain, so the latter is not of much concern. The problem occurs during startup or during large CM transients, in which case the input differential pair turns off. If not designed properly, the output swings to rails and stays there. As noted in [1], many operational amplifiers have no built-in provision to avoid these latching states. For the design in Fig. 1, a latching state will exist if $I_4 > I_2$ or $I_3 < I_1$. Thus to avoid the latching state, the CMFB loop should at least control I_1 . It is worth noting that this problem of latching states can exist even if we feed the CMFB to transistor M_2 instead of M_3 or if we had an NMOS input stage instead of a PMOS input stage.

In general it is more difficult to compensate the CMFB loop compared to the differential loop because of two additional poles in the former. The CM loop gain is given by (assuming that RHP zero due to Miller compensation is removed by the nulling resistor R_z)

$$A_{CM}(s) = \frac{A_0(1 + s/\omega_z)}{(1 + s/\omega_d)(1 + s/\omega_L)(1 + s/\omega_f)(1 + s/\omega_{cm1})(1 + s/\omega_{cm2})} \quad (2)$$

where

$$A_0 \simeq \frac{g_{m3}g_{m5}g_{m6}g_{m8}}{(g_{m6}g_{ds5}(g_{ds4} + g_{ds3}) + g_{m5}g_{ds2}g_{ds6})(g_{ds11} + g_{ds8})} * \frac{1}{2} \left(\frac{g_{m7}}{g_{m9}} \right)$$

$$\omega_d \simeq \frac{g_{m3} * A_1}{A_0 C_C}, \quad A_1 = \frac{g_{m7}}{2g_{m9}}$$

$$\omega_f = \frac{g_{m5}}{C_{gs5} + C_{sb5} + C_{db1} + C_{gd1} + C_{db3} + C_{db4}},$$

$$\omega_{cm1} = \frac{4}{R_1(4C_1 + C_{gs7})}$$

$$\omega_{cm2} = \frac{g_{m9}}{C_{gs9} + C_{db9} + C_{gs3}}, \quad \omega_L \simeq \frac{g_{m8}}{C_L}, \quad \omega_z = \frac{1}{R_1 C_1}$$

For $C_{gs7} \ll 4C_1$, $\omega_{cm1} \simeq \omega_z$ so (2) simplifies to

$$A_{CM}(s) = \frac{A_0}{(1 + s/\omega_d)(1 + s/\omega_L)(1 + s/\omega_f)(1 + s/\omega_{cm2})} \quad (3)$$

For the circuit in Fig. 1, the differential loop bandwidth is given by $\beta g_{m1}/C_C$, while $A_1 g_{m3}/C_C$ gives the CM loop bandwidth. C_C is generally chosen to compensate the differential loop optimally. Since the feedback factor (β) does not affect the CM loop bandwidth, for a design with small β , it is possible to have $A_1 g_{m3}/C_C > \beta g_{m1}/C_C$, leading to CM stability issues. The solution mentioned in [2] and widely used is to reduce the fraction of current controlled by the CMFB (reduce I_3) and hence to reduce g_{m3} . This will lead to increased DC CM error (1) and also if I_3 is made less than I_1 we will have latching states in the design.

Proposed solution: There are two contradictory requirements: for stability it is desirable to have small bandwidth, while for avoiding latching states it is desirable to have large bias currents. The proposed solution illustrated in Fig. 2b solves this problem by having two paths in the CM loop: a slow path (M'_3) and a fast path (M_3). The combination of the slow path and fast path determines the DC performance of the CM loop, while only the fast path determines the bandwidth of the loop. The slow path is created by having a series RC lowpass filter (R_2 , C_2) in the loop. The 3 dB bandwidth of this filter is set to about one-tenth of the fast path bandwidth, which ensures that the slow path is not active near unity gain bandwidth (UGB) of the loop. The bandwidth of the loop is determined by how the current I_3 is split between the fast path (I'_3) and the slow path (I''_3). Let us define $I''_3 = kI_3$ and $I'_3 = (1 - k)I_3$. If it is assumed that $\omega_{cm1} \simeq \omega_z$ as in (3), we get the following expression for the loop gain:

$$A_{CM}(s) = \frac{kA_0(1/k + s/\omega_{ps})g_{m9}}{(1 + s/\omega_d)(1 + s/\omega_L)(1 + s/\omega_f) [s^2 R_2 C_p C_2 + s C_p + s(g_{m9} R_2 + 1) + g_{m9}]} \quad (4)$$

where $\omega_{ps} = 1/(R_2 C_2)$ and $C_p = C_{gs9} + C_{db9} + C_{gs3}$. With $g_{m9} R_2 \gg 1$ (4) simplifies to

$$A_{CM}(s) \simeq \frac{kA_0(1/k + s/\omega_{ps})}{(1 + s/\omega_d)(1 + s/\omega_L)(1 + s/\omega_f) (1 + s/\omega_{pf})(1 + s/\omega_{ps})}$$

$$= \frac{A_0}{(1 + s/\omega_d)(1 + s/\omega_L)(1 + s/\omega_f)} \times \left(\frac{k}{(1 + s/\omega_{pf})} + \frac{1 - k}{(1 + s/\omega_{pf})(1 + s/\omega_{ps})} \right) \quad (5)$$

where $\omega_{pf} = g_{m9}/C_p$.

Owing to the multipath scheme, the overall transfer function (4) has an additional pole and zero at low frequencies. Since both the pole and

zero are at low frequencies compared to the loop bandwidth, the overall response at high frequencies is just due to the fast path. The loop bandwidth is now given by $A_1 g_{m3}' / C_C = A_1 k g_{m3} / C_C$.

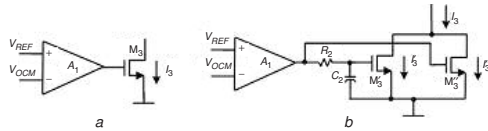


Fig. 2 Traditional CMFB and multipath CMFB schemes
a Traditional
b Multipath

The effect of having a pole-zero doublet on the settling response of the loop has been analysed in [3]. If the doublet is at low frequency compared to the loop bandwidth, the magnitude of the slow-settling component is small, and this is guaranteed in the design by choice of the lowpass filter ($R_2 C_2$). As the pole-zero doublet spacing increases the magnitude of the slow-settling component increases. In this design zero will appear at $1/k$ times the pole frequency, so for a practical design k should not be too small ($k > 0.2$). For our design k was chosen as 0.5. The slow-settling components become visible only if we desire very high settling accuracies, which is generally not the case with CM feedback circuits.

Another aspect, which deserves mention, is the fact that noise due to the R_2 in the filter appears as CM noise. Only a very small fraction ($< 1\%$) of this noise appears as differential noise as long as the matching between the positive and the negative branch of the amplifier is reasonable.

An additional advantage of using the multipath approach is the increase in the DC transconductance gain and hence the DC accuracy of the CM loop, which may be critical in some designs [4]. This is a direct consequence of controlling a larger fraction of bias currents by the CMFB loop.

Simulation results: Two amplifiers were designed in $0.5 \mu\text{m}$ CMOS technology, one with a multipath CMFB loop ($k = 0.5$) and the other with conventional design. The same amount of bias current is controlled in both CMFB loops ($> I_1$ to avoid latching states). Fig. 3 compares the CM loop AC response of both amplifiers. The UGB in the multipath approach reduces from 100 to 65 MHz while the phase margin (PM) improves from 24° to 50°

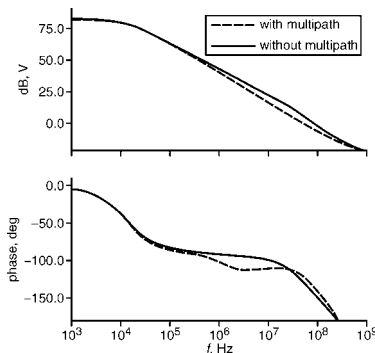


Fig. 3 AC response for CMFB loop
Traditional CMFB (UGB = 100 MHz, PM = 24°) and multipath CMFB with $I_3' = I_3'' = I_3/2$ (UGB = 65 MHz, PM = 50°)

Fig. 4 shows the CM output with a 400 mV step on the CM control signal. The conventional CMFB output exhibits ringing owing to poor phase margin. Another observation is that there are no slow-settling components visible in the output with the multipath CMFB scheme.

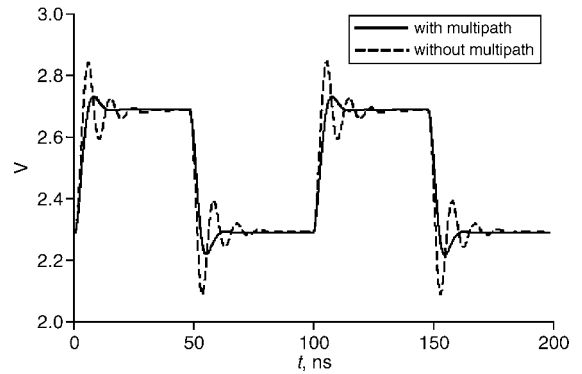


Fig. 4 Settling of common-mode output with 400 mV step on V_{REF}

Conclusions: It has been shown that there is a need to control a large fraction of current by a CM loop in two-stage amplifiers to avoid latching states, which inevitably leads to larger CM loop bandwidth. A multipath CMFB approach has been proposed, which allows controlling a larger current but at the same time maintains a low bandwidth. This makes it easy to compensate the CM loop.

© The Institution of Engineering and Technology 2006
15 February 2006

Electronics Letters online no: 20060454
doi: 10.1049/el:20060454

A.K. Gupta, V. Dhanasekaran and E. Sanchez-Sinencio (Department of Electrical Engineering, Texas A&M University, College Station, TX, USA)

E-mail: ak Gupta@ee.tamu.edu

K. Soundarapandian (High Performance Analog, 12500 Texas Instruments, Dallas, TX, USA)

References

- Banu, M., Khoury, J.M., and Tsividis, Y.: 'Fully differential operational amplifiers with accurate output balancing', *IEEE J. Solid-State Circuits*, 1988, **23**, (6), pp. 1410–1414
- Gray, P.R., et al.: 'Analysis and design of analog integrated circuits' (Wiley, New York), 2001, 4th edn. Chap. 12
- Kamath, Y.B., Meyer, R.G., and Gray, P.R.: 'Relationship between frequency response and settling time of operational amplifiers', *IEEE J. Solid-State Circuits*, 1974, **9**, pp. 347–352
- Luh, L., Choma, J., and Draper, J.: 'A continuous-time common mode feedback circuit (CMFB) for high impedance current-mode applications', *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, 2000, **47**, (4), pp. 363–369