

FULLY INTEGRATED FREQUENCY SYNTHESIZERS: A TUTORIAL

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Frequency synthesizer is a key building block of fully-integrated wireless communications systems. Design of a frequency synthesizer (FS) requires the understanding of not only the circuit-level but also of the transceiver system-level considerations. The FS design challenge involves strong trade-offs, and often conflicting requirements. In this tutorial, the general implementation issues and recent developments of frequency synthesizer design are discussed. Simplified design approach should provide readers with sufficient intuition for fast design and troubleshooting capability. Open problems in this FS field are briefly discussed.

Keywords: Analog integrated circuits; CMOS/BiCMOS RF; frequency synthesizer; phase-locked loop

1. Introduction

Wireless communications gained popularity as the electronics industry introduced accessible consumer products leading the emerging market. The most effective way to save production cost and to minimize form factor has been the monolithic implementation of the entire RF transceiver on a single chip. In a fully integrated system, the frequency synthesizer design represents a major challenge since the circuit has to meet stringent and conflicting requirements.

A frequency synthesizer (FS) is a device capable of generating a set of signals of given output frequencies with very high accuracy and precision from a single reference frequency. The signal generated at the output of the frequency synthesizer is commonly known as local oscillator (LO) signal, since it is used in communication systems as the reference oscillator for frequency translation as shown in Fig. 1. The

reference signal at high frequency is used to downconvert the incoming signal into a lower frequency where it can be processed to extract the information it is carrying. The same reference signal can be used to upconvert a desired message to an RF frequency, such that it can be transmitted over the medium.

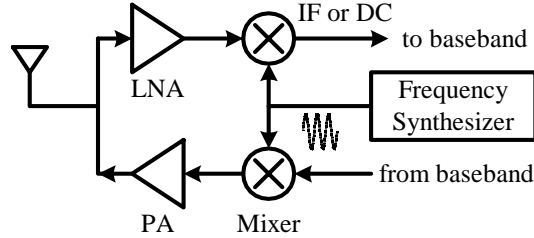


Fig. 1. The role of a frequency synthesizer in a communication transceiver

Normally, the FS output signal is a sinusoidal tone plus harmonic tones that are added due to non-linearities. Fundamentally, the whole frequency synthesizer system is designed to ensure the accuracy of its output frequency under any condition. In fact, the accuracy requirements are so tight that the accuracy are in the order of tens of ppm. For example, the final frequency accuracy in Wireless LAN 802.11a standard is 20 ppm, which translates into 116 kHz for a carrier frequency of 5.805 GHz.¹ In addition to the frequency accuracy, the spectral purity of the output signal and the settling time determine the performance merits of a frequency synthesizer.

This tutorial discusses the general design considerations and recent developments of frequency synthesizers design. Section 2 studies a methodology of interpreting communication standards into circuit specifications as a top-down design strategy. Section 3 and 4 covers the details of conventional frequency synthesizer. Section 5 summarizes the recent development of advanced techniques to improve the performance of frequency synthesizers. The tutorial assumes the reader has a basic understanding of PLL operation² and builds on that knowledge to describe more detailed design issues particular to wireless communications frequency synthesizers.

2. Interpreting Specifications

The detailed specifications for the transistor-level design of frequency synthesizers are not readily available from the standard, but are embedded within the description of the requirements for the communication system. Also, particular characteristics of the system design set constrains in the specifications of the frequency synthesizer. For example, even though the RF frequencies are set for a given standard, the selection of a given intermediate frequency (IF) determines the required output frequency range of the synthesizer. Table 1 is used to illustrate the information in some standard documents, that is relevant to frequency synthesizer design. Full details of several wireless communication standards can be found in the literature.^{1,3,4,5}

Table 1. Short range wireless communications standards

	Bluetooth	802.11a	802.11b	802.11g
Bit rate	1 Mbps	54 Mbps	11 Mbps	54 Mbps
Sensitivity	-70 dBm	-82 dBm	-76 dBm	-76 dBm
Frame Error Rate	10^{-3} (BER)	10^{-5}	8×10^{-2}	8×10^{-2}
Band (MHz)	2400–2479	5180–5805	2412–2472	2412–2472
Channel Spacing	1 MHz	20 MHz	5 MHz	20 MHz
Accuracy	± 75 kHz ^a	± 20 ppm	± 25 ppm	± 25 ppm
Settling	$< 259 \mu s$	$224 \mu s$	$224 \mu s$	$224 \mu s$
Interference	+40 dB at 3 MHz	+32 dB at 40 MHz	+35 dB at 25 MHz	+35 dB at 25 MHz

^aEquivalent to 30 ppm

2.1. Frequency Band and Tuning Range

Every communication standard utilizes a specific frequency band in the spectrum of electro-magnetic waves according to the usage models, and the regulations of the governing body. For instance, the 2.4 GHz Industrial-Scientific-Medical (ISM) band is most popular for short range communication standards such as Bluetooth and Wireless LAN, because the usage of the ISM band is free and the frequency is high enough to limit the reach of the transmitted signal.

In phase-locked loop (PLL) based frequency synthesizers, the tuning range of the voltage controlled oscillator (VCO) determines the limits on the overall system tuning range. The tuning range of the VCO should be much larger than the frequency band of interest since it will have large range of uncertainty due to process variations and modelling uncertainties. A 20% deviation in either inductance or capacitance in a LC oscillator will result in more than 10% error in the output frequency.

Other factors, such as the linear range at the output voltage of the charge pump (CP) can further limit the tuning range of the synthesizer. The design should account for the limits of both, the VCO control voltage and CP output linear range to ensure the synthesizer can operate properly. If the CP cannot provide the designed current amplitude for certain output voltages, the system transfer function loses its gain and may become unstable. The voltage swing can be severely limited if the charge pump has a cascode output stage for improved output impedance.⁶

2.2. Channel Agility and Settling Time

Whenever the transmission or reception channel switches in a communication system, the transceiver must change its local oscillator frequency to synchronize with the received/transmitted signal. Since most frequency synthesizers utilize a feedback mechanism to control the accuracy of the output frequency, and minimize the

difference between the output and the target frequency, the switching of the output frequency cannot be instantaneous. The output frequency approximately follows the step response of a second order system for very small phase errors. This condition holds only when the frequency step is much smaller than the center frequency, as in narrow-band systems. For large frequency steps in wide-band systems, the response will slow down due to very non-linear behavior associated with large phase errors.

For instance, in the Bluetooth standard, the frequency synthesizer settling time is not clearly defined, but it can be calculated from the relationship between the time slot length and the packet length. Since the Bluetooth standard uses frequency hopping at 1600 hops per second, the transceiver is only allowed to transmit within a time slot of $T_{slot} = 625 \mu\text{s}$. The length of a standard single packet to be transmitted in a time slot is 366 bit long, corresponding to $T_{pkt} = 366 \mu\text{s}$. Thus the downtime between two consecutive time slots is,

$$T_{down} = T_{slot} - T_{pkt} = 259 \mu\text{s} \quad (1)$$

The transceiver must complete a transition between transmitting and receiving during the T_{down} period, including the settling of the frequency synthesizer. Note that the settling time of the frequency synthesizer is only a fraction of the turnaround time because the blocks following the mixer, such as variable gain amplifier (VGA), also need certain amount of time to settle once the frequency synthesizer is settled.

Wireless LAN standards explicitly specify channel agility to be 224 μs in the standard section 18.4.6.12. A frequency synthesizer is considered to be settled when the center frequency is stable within the frequency accuracy limit, which is $\pm 60 \text{ kHz}$ for the case of 802.11b.

2.3. Spectral Purity

The spectral purity of the local oscillator is usually not explicitly specified in most of the communication standards. Instead, phase noise and spurious signal specifications are usually derived from adjacent channel interference requirements.⁶ The strongest adjacent channel interferences of several popular short-range standards are listed in Table 1.

The effect of phase noise and adjacent channel interference is shown in Fig. 2. While the signal (P_{Sig}) is downconverted to DC or IF by the LO signal (P_{LO}), the interference (P_{Int}) is also downconverted to DC or IF by the phase noise (P_N) and is added to the signal of interest. Since the phase noise is a random process, the effective bandwidth (P_{BW}) is added to calculate the total power. The signal to noise ratio (SNR) of the baseband signal is the difference of the power of the two, and it must be larger than the minimum SNR required to meet the receiver bit

error rate (BER) requirement.

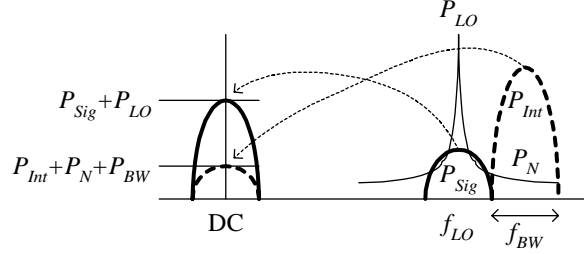


Fig. 2. The effect of phase noise and interference

$$SNR = (P_{Sig} + P_{LO}) - (P_{Int} + P_N + P_{BW}) > SNR_{min} \quad (2)$$

After rearrangement,

$$P_N - P_{LO} < (P_{Sig} - P_{Int}) - P_{BW} - SNR_{min} \quad (3)$$

where $P_N - P_{LO}$ denotes the phase noise requirement in dBc – a power spectrum density relative to the carrier power. For example, from Table 1, Bluetooth standard specifies an interferer of +40 dB at 3 MHz away from the desired signal. The channel bandwidth is 1 MHz, which translates into $P_{BW} = 10 \log 10^6 = 60$ dB. The minimum SNR requirement for a BER of 10^{-3} is 18 dB, which can be determined from system level baseband simulations.^a Substituting these numbers in Eq. (3), the phase noise requirement is -118 dBc at 3 MHz from carrier. This calculation assumes the phase noise is white within the channel bandwidth. A realistic design goal should include some margin from the calculated value.

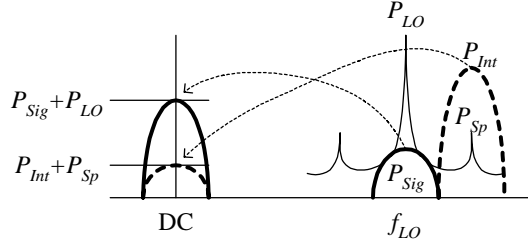


Fig. 3. The effect of reference spur and interference

Reference spur can be a especially serious problem if the system uses narrow channel spacing and the spur coincides with the adjacent channels as shown in Fig. 3. This kind of situation can happen when implementing Bluetooth transceivers with an integer-N type frequency synthesizer. The calculation is similar to the one

^aFor this tutorial, SytemViewTM software is used to simulate GFSK coded baseband signal for Bluetooth system. The BER of the final signal is measured while sweeping the additional noise power.

previously presented for phase noise case except that the interference is downconverted by spurious signal, which is considered as a single tone. With the SNR of the baseband signal being,

$$SNR = (P_{Sig} + P_{LO}) - (P_{Int} + P_{Sp}) > SNR_{min} \quad (4)$$

After rearrangement,

$$P_{Sp} - P_{LO} < P_{Sig} - P_{Int} - SNR_{min} \quad (5)$$

where $P_{Sp} - P_{LO}$ denotes the power of spurious signal in dBc, relative to the carrier power. For example, Bluetooth standard specifies an interferer of +30 dB at 2 MHz away from the desired signal. The reference spur can be also at 2 MHz away from the carrier if the frequency of the reference signal is 2 MHz. The minimum SNR requirement is 18 dB, same as the previous example. Substituting the numbers in Eq. (5), the spurious signal requirement results in -48 dBc at 2 MHz from carrier.

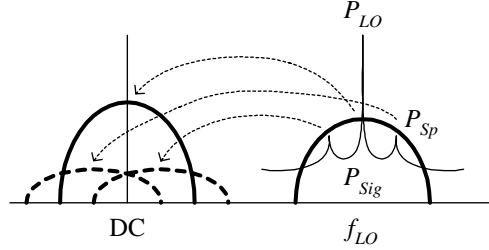


Fig. 4. The effect of reference spur in 802.11b system

In the case of Wireless LAN 802.11b as shown in Fig. 4, the reference spur can fall *within* the received signal, but not in the adjacent channel because the channel bandwidth can be larger than the reference frequency. System level simulations are required to determine the specific level of spur that degrades the receiver BER below the given specification.^b Simulation results are presented in Fig. 5. The SNR of the input signal swept from 10.5 dB to 14 dB, while four different spur power of -34 , -28 , -22 , and -16 dB are degrading the input signal. The result shows that the reference spur must be at least 25 dB below the carrier signal to keep a BER better than 10^{-5} when the input SNR is 12 dB. This requirement also needs

^bThe CCK coded baseband signal of 802.11b system is simulated using SytemViewTM software. The baseband signal is up-converted by 2 MHz and then added to the original baseband signal. The degradation of the final signal is measured in terms of BER.

additional margin for a realistic design.

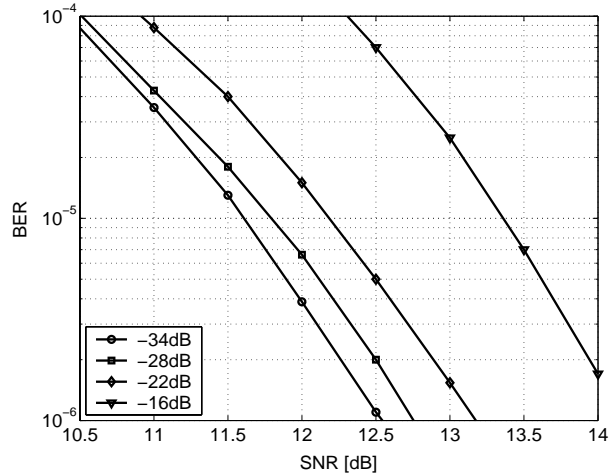


Fig. 5. The effect of reference spur at 2 MHz in 802.11b system

Table 2 summarizes the mapping relationship between the communication standard and the building block specification. It is possible for several aspects of the standard to be mapped into a single specification, and vice versa. For illustration purpose, a specific example for 802.11b standard is given in separate columns.

Table 2. Summary of specification mapping

Standard		Specification	
General	802.11b	General	802.11b
Frequency Band	2412–2472 MHz	Tuning range	2412–2472 MHz
Channel spacing	5 MHz	Tuning step	1 MHz
Hopping rate	N/A	Settling time	224 μ s
Packet structure	N/A	Settling time	N/A
Interference	+35 dB at 25 MHz	Phase noise	-126 dBc at 25 MHz
Interference	N/A	Spur rejection	-25 dBc at 2 MHz

3. Types of Frequency Synthesizers

3.1. PLL based Integer-N Synthesizer

The most popular technique of frequency synthesis is based on the use of a phase-locked loop (PLL). The loop is synchronized or locked when the phase of the input signal and the phase of the output from the frequency divider are aligned. As shown in Fig. 6, the output of the VCO in the integer-N synthesizer is divided and phase-locked to a stable reference signal. Once the loop is locked, the output frequency

equals the reference frequency times N .

$$f_{out} = N \cdot f_{REF} \quad (6)$$

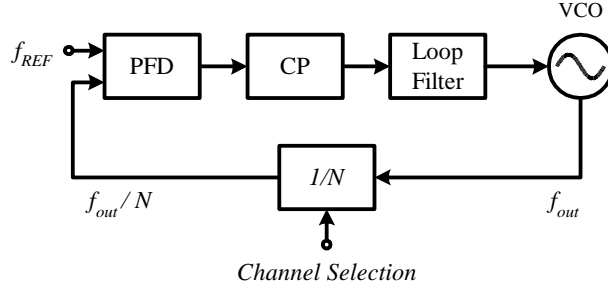


Fig. 6. Integer-N architecture

Integer-N architecture is the preferred solution for minimizing power consumption and die area due to its simplicity. The integer-N architecture, however, lacks the flexibility of arbitrarily choosing f_{REF} as is possible in more complex architectures. Since f_{REF} is fixed by channel spacing requirements, the loop bandwidth can be severely limited, especially since it has to be significantly lower than f_{REF} for stability considerations.

Although, the integer-N synthesizers can generate output frequencies in steps of f_{REF} , the channel spacing is not necessarily equal to f_{REF} . The maximum possible f_{REF} can be calculated as follows: First, the channel frequencies must be integer multiples of f_{REF} as shown in Eq. (6), but at the same time the channel spacing also has to be an integer multiple of f_{REF} . To satisfy both conditions, the f_{REF} has to be the greatest common divisor (GCD) of the channel frequency and the channel spacing. For example, Wireless LAN 802.11b standard specifies channels from 2412 MHz to 2472 MHz in steps of 5 MHz. Thus, the maximum possible f_{REF} is $GCD(2412 \text{ MHz}, 5 \text{ MHz}) = 1 \text{ MHz}$. For a different example, Wireless LAN 802.11a standard specifies a channel at 5805 MHz and a step of 20 MHz. In this case, the maximum possible f_{REF} is $GCD(5805 \text{ MHz}, 20 \text{ MHz}) = 5 \text{ MHz}$.

3.2. PLL based Fractional-N Synthesizer

An inherent shortcoming of the integer-N synthesizer is the limited option for the reference frequency, f_{REF} , because of the integer-only multiplication. A fractional-N synthesizer architecture solves this problem by allowing fractional feedback ratios. Shown in Fig. 7, the fractional-N synthesizer has a dual modulus divider that can switch its division ratio between N and $N + 1$. By dividing the VCO frequency by N during K VCO cycles and $N + 1$ during $(2^k - K)$ VCO cycles, it is possible to make the average division ratio equal to $N + K/2^k$, assuming a k bits accumulator controlling the prescaler. Thus,

$$f_{out} = (N + \alpha) \cdot f_{REF} \quad , \text{ where } 0 < \alpha < 1 \quad (7)$$

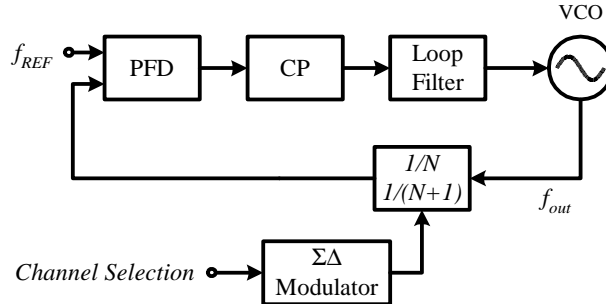


Fig. 7. Fractional-N architecture

However, if the division modulus is switched periodically, the output is modulated by the beat frequency of the fractional modulus. It can be shown that the output spectrum has tones at αf_{REF} , $2\alpha f_{REF}$ and so on, relative to the carrier frequency. These are fractional spurs and can be problematic since they are very close to the carrier.

The fractional spurs can be reduced by breaking the regularity of the division modulus switching period, effectively making the beat frequency randomized. A dithering mechanism using $\Sigma\Delta$ modulator can not only randomize the beat frequency, but shape the noise spectrum so that it has more power at higher frequency. The high frequency quantization noise is filtered by the loop filter of the PLL. A combination of the order of the $\Sigma\Delta$ modulator and loop filter order can reduce the high frequency quantization noise at levels that make the effect of the noise negligible.⁷

3.3. Direct Digital Synthesizer (DDS)

A fundamental reason that a feedback control loop is used in the implementation of frequency synthesizers is because the relationship between the control voltage and the output frequency of a VCO is unpredictable and subject to variations from unwanted excitations. If a VCO's output signal frequency were always predictable with no variation, there would be no need to use feedback control to correct the error in frequency. The output of the VCO would be used directly as the final output of the frequency synthesizer. In this hypothetical system, there would be no problem of stability and settling time. The settling time would be only limited by the gate delay of the channel selection input.

DDS generates its output signal from the digital domain and converts it in analog waveform through a digital-to-analog converter (DAC) and filtering as shown in Fig. 8. Since the waveform is directly shaped from the amplitude values from a read-only-memory (ROM), it doesn't require feedback and it has all the advantages of the hypothetical system previously described. In addition, it has other advantages such as low phase noise and possibility of direct digital modulation. The DDS is

a suitable choice when the carrier frequency has to be settled very fast with very low phase noise.⁸ The application of the FS is to generate frequency-hopped carrier signals for NMT-900 cell phone standard. Another usage of DDS is when extremely fine frequency resolution is required.⁹ This synthesizer covers a bandwidth from DC to 75 MHz in steps of 0.035 Hz with a switching speed of 6.7 ns.

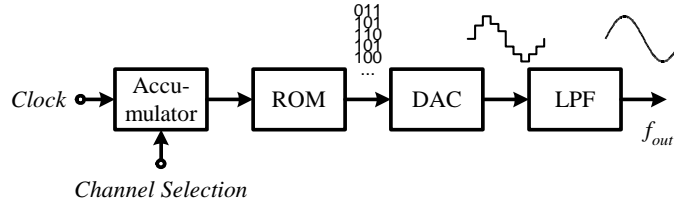


Fig. 8. Direct digital synthesizer block diagram

The most serious shortcoming of DDS is speed: the clock of the digital circuitry has to be at least twice as high as the output frequency. Operating a ROM and a DAC at 4.8 GHz to generate 2.4 GHz output signals can be challenging in current technologies, if at all possible, and power consumption will be prohibitively high. In addition, large quantization noise and harmonic distortion of high speed DACs can degrade the spectral purity of the output signal. Using an analog mixer to upconvert a low frequency synthesized signal, in order to generate high frequency outputs without an excessively high frequency clock, has been reported in literature.¹⁰ However, it is a costly solution since it needs an extra analog PLL and high frequency mixers.

4. Phase Locked Loop (PLL) Design

This section covers the fundamentals of PLL design for frequency synthesizers. Rather than focusing on circuit implementation issues, system level designs such as loop transfer function and stability considerations are addressed with insightful observations. Extensive PLL design techniques can be found in the literature.^{2,11,12}

4.1. Charge-pump PLL

Virtually all of the PLL-based frequency synthesizers utilize a charge-pump PLL that was first introduced by Gardner.¹³ Charge-pump PLL has important advantages that make it suitable for the implementation of frequency synthesizers. These advantages include:

- (i) The operation of phase frequency detector (PFD) makes the frequency acquisition range not limited by loop bandwidth but only by VCO tuning range.
- (ii) Due to poles at the origin, charge-pump PLL has infinite open-loop gain at DC, which make the static phase error to be ideally zero.

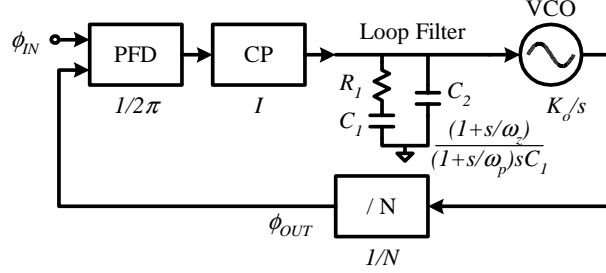


Fig. 9. Charge-pump PLL block diagram and linear approximation

A simplified block diagram of the charge-pump (CP) PLL is shown in Fig. 9. The fundamental process of operation is as follows. First, the VCO oscillates at its natural frequency assuming the control voltage is arbitrary at the beginning. The PFD compares the phase difference between the reference signal ϕ_{IN} and the VCO output divided by the frequency divider, ϕ_{OUT} . The output of the PFD is a series of pulses whose duty cycle is proportional to the phase difference $\phi_{IN} - \phi_{OUT}$. The CP converts the voltage pulses into current pulses with a predetermined amplitude I . The loop filter converts the current pulses into a low-pass filtered voltage signal that controls the frequency of the VCO. If the feedback is negative, the error between ϕ_{IN} and ϕ_{OUT} gradually become smaller and smaller until $\phi_{IN} = \phi_{OUT}$. In this state the loop is referred to be *locked*. Once the loop is locked, the frequency of the VCO output is equal to the frequency of the reference multiplied by the feedback factor N .

The process of locking is not instantaneous because the loop has a limited bandwidth. The transfer function of the loop has to be studied to estimate the behavior of the loop during its transient operation. Since the operation of the PFD and CP is performed in the discrete-time domain, the complete transfer function becomes complicated due to the z-transform representation. A more intuitive equation can be obtained by assuming the phase error is small. With this assumption, the PFD and CP are modelled as simple gain blocks, $1/2\pi$ and I respectively, as shown in Fig. 9.

The linear approximation gives two critical equations useful for the initial design of a PLL. The first equation is an open-loop transfer function which is ϕ_{OUT}/ϕ_{IN} assuming the loop is opened between the frequency divider and the PFD.

$$H_{open}(s) = \frac{\phi_{OUT}}{\phi_{IN}} = \frac{K_D K_o (1 + s/\omega_z)}{(1 + s/\omega_p) s^2} \quad (8)$$

where $K_D = I/(2\pi C_1 N)$, $\omega_z = 1/(R_1 C_1)$ and $\omega_p \simeq 1/(R_1 C_2)$. The open-loop transfer function is important because its phase margin indicates how stable the system will be after the loop is closed. Note that there are two poles at the origin and a stabilizing zero is required to compensate for them. Details of PLL stability are covered in section 4.2.

The second equation is a closed-loop transfer function ϕ_{IN}/ϕ_{OUT} . It can also be calculated from $H_{open}(s)/(1 + H_{open}(s))$.

$$H_{closed}(s) = \frac{\phi_{OUT}}{\phi_{IN}} = \frac{1 + s/\omega_z}{1 + s/\omega_z + s^2/(K_D K_o) + s^3/(\omega_p K_D K_o)} \quad (9)$$

For simplicity, it is assumed that ω_p is placed at very high frequency with respect to the natural frequency $\omega_n = \sqrt{K_D K_o}$, then the transfer function becomes second order.

$$H'_{closed}(s) \simeq \frac{1 + s/\omega_z}{1 + s/\omega_z + s^2/(K_D K_o)} \quad (10)$$

The step response of the closed-loop transfer function shows the locking transient, and settling time performance can be determined from the transient waveform. Analytic solution of the settling time can be derived from the second order transfer function. The details of the settling analysis is covered in section 4.3.

4.2. Stability

As in any feedback system, stability is one of the most important aspects of the design considerations of frequency synthesizers. A potentially unstable synthesizer will generate an output signal whose frequency does not converge but *oscillates* between certain frequency limits. The unstable output signal appears similar to narrow-band FM modulated signal.

There are two sources for the stability limit in charge-pump PLL. The first comes from the fact that the operation of PFD and CP is in the discrete-time domain. Loop bandwidth has to be carefully chosen so that the linear approximation is not violated i.e. $\omega_c < \omega_{REF}$. The second comes from the two poles at the origin in the open-loop transfer function. A stabilizing zero can compensate for the effect of the double poles at crossover frequency. More detailed analysis on stability limit follows.

First, the charge-pump PLL has a critical stability limitation due to the discrete nature of the PFD and CP output. The PLL operates as a sampled system and not as a straightforward continuous-time circuit. It is known that a sampled second-order PLL will become unstable if the loop gain is made so large that the bandwidth becomes comparable to the sampling frequency. Limited loop gain sets upper boundary of the loop bandwidth obtainable for a given input reference frequency. Gardner's stability limit states that:¹³

$$\omega_n^2 < \frac{\omega_{REF}^2}{\pi(\pi + \omega_{REF}/\omega_z)} \quad (11)$$

The relationship between the natural frequency (ω_n) and the loop bandwidth (ω_c) is approximately:

$$\omega_c \simeq \omega_n^2/\omega_z \quad (12)$$

for critically damped and overdamped system. Substituting Eq. (12) into Eq. (11), it can be rewritten as:

$$\omega_c < \frac{\omega_{REF}}{\pi(1 + \pi\omega_z/\omega_{REF})} \quad (13)$$

which indicates that the loop bandwidth (ω_c) has to be significantly lower than the frequency of the reference input signal (ω_{REF}). Commonly ω_c is chosen below one-tenth of ω_{REF} to guarantee stability. Another important factor to consider when determining the loop bandwidth is the size of the capacitors to realize the bandwidth. If the loop bandwidth is too narrow, the size of the capacitors can be excessively large to be implemented in a fully-integrated solution. Using dual-pass active filter¹⁴ or impedance multiplier¹⁵ are proposed to emulate a large capacitance without consuming huge die area. Their application is limited to a multiplication factor no more than 20 due to uncertainties from mismatch. Furthermore, the additional active device in the signal path can degrade phase noise and increase reference spurs due to leakage current.

The second stability limit comes from the open-loop transfer function. As has already been shown in Eq. (8), the open-loop transfer function of a charge-pump PLL has two poles at the origin, which makes the loop inherently unstable. A zero should be placed at a lower frequency than the crossover frequency to make the phase margin large enough ($> 45^\circ$). Since the zero reduces the slope of the magnitude response, an additional pole at a higher frequency than the crossover frequency is also required to maintain adequate spurious signal rejection.

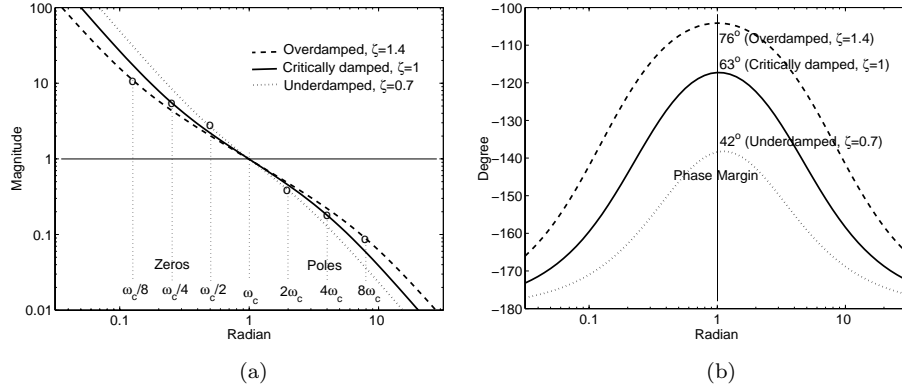


Fig. 10. The effect of pole/zero placement on phase margin (a) Pole/zero are placed 2, 4 and 8 times crossover frequency ω_c . (b) Phase margin increases from 42° to 76° as pole/zero are placed farther apart.

Three examples of different pole/zero placements are shown in Fig. 10. The open-loop transfer functions of those three examples referred to Eq. (8) are

$$H_{under}(s) = \frac{1 + 2s}{2(1 + s/2)s^2} \quad (14)$$

$$H_{critical}(s) = \frac{1 + 4s}{4(1 + s/4)s^2} \quad (15)$$

$$H_{over}(s) = \frac{1 + 8s}{8(1 + s/8)s^2} \quad (16)$$

When a zero is located at $1/4$ of the crossover frequency (w_c) and a pole is placed at 4 times of w_c , the loop is critically damped with the damping ratio of 1. A phase margin of 63° can be achieved. When the zero is at $w_c/2$ and the pole is at $2w_c$, the loop is underdamped with the damping ratio of 0.707. With an underdamped loop, the phase margin is lowered to 42° and the transient signal overshoots. When the zero is at $w_c/8$ and the pole is at $8w_c$, the loop is overdamped with a damping ratio of 1.414. With an overdamped loop, the phase margin is increased to 76° but the settling time is degraded due to slow response.

Normally a critically damped loop works best for a typical frequency synthesizer design. A slightly underdamped loop can be beneficial to keep the optimal settling time when the process variation is significant. When using an underdamped loop, the overshoot has to be kept within the dynamic range of the charge-pump and the tuning range of the VCO. If the dynamic range of the charge-pump is severely limited, as in a low-voltage design, an overdamped loop can be a better choice to minimize the overshoot. However, the loop bandwidth has to be increased to compensate for the degraded settling time due to overdamping.

4.3. Settling time

Settling time is another important performance metric that is directly related to the loop transfer function. Settling time determines how fast the frequency synthesizer can change the frequency of its output signal.

An analytical solution for the settling time can be obtained from the step response of the closed-loop transfer function, see Eq. (10). Settling time is a function of the natural frequency ($\omega_n = \sqrt{K_D K_o}$) and the damping factor ($\zeta = \omega_n/(2\omega_z)$). It can be shown that

$$t_s \simeq \begin{cases} \frac{1}{\zeta\omega_n} \ln \frac{\Delta f}{\alpha f_o \sqrt{1-\zeta^2}} & \text{if } \zeta < 1 \text{ (under)} \\ \frac{1}{\zeta\omega_n} \ln \frac{\Delta f}{\alpha f_o} & \text{if } \zeta = 1 \text{ (critical)} \\ \frac{1}{(\zeta - \sqrt{\zeta^2 - 1})\omega_n} \ln \frac{\Delta f(\sqrt{\zeta^2 - 1} + \zeta)}{2\alpha f_o \sqrt{\zeta^2 - 1}} & \text{if } \zeta > 1 \text{ (over)} \end{cases} \quad (17)$$

where f_o is the frequency from which the synthesizer starts the transition, Δf is the amount of frequency jump, and α is the settling accuracy. As the loop bandwidth ω_c increases, the settling time gets shorter if the damping ratio is fixed. The effect of the damping ratio on settling time is shown in Fig. 11. It is a plot of Eq. (17) with ω_c fixed but not ω_n , which is more realistic in the sense of design procedure. In this condition, the settling time is fastest when the loop is critically damped, and further underdamping does not improve the settling time. Note that the analytic solution in Eq. (17) is only an approximated result for the second-order closed-loop

transfer function, but not for the third-order one. Since Eq. (10) does not take into account the effect of the additional pole, the actual settling time is longer than the analytic solution may suggest.

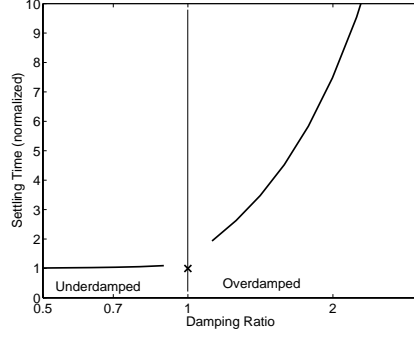


Fig. 11. Settling time vs. damping factor for a second-order PLL

The transient step responses of the third-order transfer functions are shown in Fig. 12(a). The closed-loop transfer functions of the examples are:

$$H_{under}(s) = \frac{1 + 2s}{1 + 2s + 2s^2 + s^3} \quad (18)$$

$$H_{critical}(s) = \frac{1 + 4s}{1 + 4s + 4s^2 + s^3} \quad (19)$$

$$H_{over}(s) = \frac{1 + 8s}{1 + 8s + 8s^2 + s^3} \quad (20)$$

Underdamping is not desirable since it increases overshoot in transient response while not improving settling time performance considerably. The overshoot should be limited within the dynamic range of the charge-pump output, otherwise the settling time performance will be degraded.

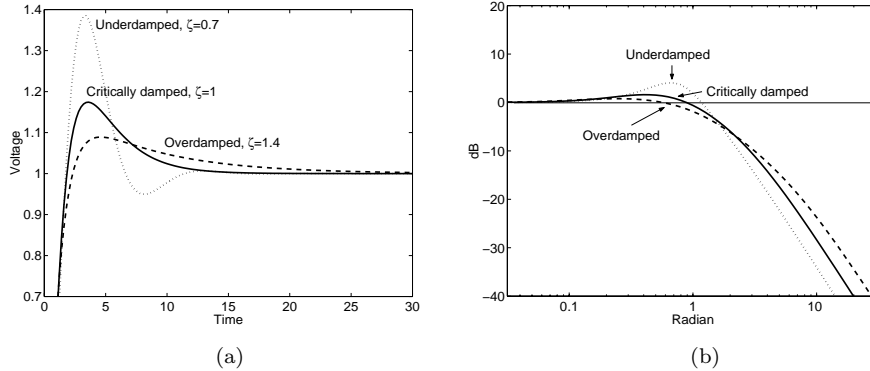


Fig. 12. Third-order closed loop characteristics (a) Transient response of underdamped, critically damped and overdamped system (b) Magnitude plot of the closed-loop transfer function shows peaking in underdamped system.

The overshoot in transient response also translates into gain peaking in the frequency domain. Fig. 12(b) shows that an underdamped system has excessive gain peaking due to the stabilizing zero. The gain peaking amplifies the phase noise of the reference signal at the output of the frequency synthesizer. It is recommended to use an overdamped system if the close-in phase noise of the reference signal has considerable effect on the receiver performance.

Finally, the trade-offs of design choices are summarized in Table 3. Loop bandwidth and damping ratios have to be determined carefully, depending on the requirement of the target application, since they improve some aspects of the performance, and deteriorate others at the same time.^c

Table 3. Summary of PLL design trade-offs

	Loop bandwidth	Damping
Faster settling	wide	under
Better stability	narrow	over
Lower phase noise	wide	N/A
Better spur rejection	narrow	N/A
Low jitter peaking	N/A	over
Low overshoot	N/A	over
Smaller capacitor size	wide	N/A

4.4. WLAN 802.11b Design Example

In this section, an example of the design procedure of the frequency synthesizer compliant for Wireless LAN 802.11b standard is presented. The procedure details the considerations for stability and settling time of loop filter design. The same procedure can be applied to different communication standards with minimal modifications.

- (i) The first step is to determine the reference frequency f_{REF} . For 802.11b standard, the output frequency must cover the range from 2412 MHz to 2472 MHz in steps of 5 MHz. If the quadrature outputs are to be generated by a divide-by-two circuit, the VCO output frequency has to be twice the requirement. Now the system must cover the range from 4824 MHz to 4944 MHz in steps of 10 MHz. Since $GCD(4824, 10) = 2$, the maximum f_{REF} possible is 2 MHz.

^cFor instance, in a frequency synthesizer design, the loop bandwidth is $f_c = 830\text{kHz}$ and the damping factor is $\zeta = 0.75$, while the reference frequency is $f_{REF} = 11.75\text{MHz}$.¹⁶ Since the loop bandwidth is close to the maximum of the Gardner's limit and the damping is underdamped, the PLL shows a fast settling time performance of $40\ \mu\text{s}$. However, stability of the system is easily disturbed during the measurement and the transient response waveform shows a large overshoot and ringing. In another design example, the loop bandwidth is $f_c = 45\text{kHz}$ and the damping factor is $\zeta = 1$, while the reference frequency is $f_{REF} = 26.6\text{MHz}$. Relatively low loop bandwidth leads to a slow settling time of $250\ \mu\text{s}$.¹⁴

- (ii) From the Gardner's stability limit, the loop bandwidth ω_c has to be well below ω_{REF} . Considering that the settling time requirement is relatively relaxed, it is beneficial to make the loop bandwidth very narrow to reduce reference spur. Let $\omega_c = 2\pi \times 30\text{kHz}$, then the loop bandwidth is 66 times below f_{REF} .
- (iii) For optimal settling time performance, make the loop critically damped. The damping ratio is $\zeta = 1$.
- (iv) From Eq. (10) and Eq. (12), the natural frequency is $\omega_n = \omega_c/(2\zeta) = 2\pi \times 15\text{kHz}$.
- (v) Now that ω_n and ζ are determined, the settling time can be estimated from the closed form Eq. (17). Using $f_o = 4824$, $\Delta f = 120$ and $\alpha = 25 \times 10^{-6}$, the estimated settling is $t_s = 73 \mu\text{s}$. It is faster than the required $224 \mu\text{s}$ by a good margin.
- (vi) From the loop bandwidth and the damping factor, the location of the stabilizing zero can be determined as $\omega_z = \omega_c/(4\zeta^2) = 2\pi \times 7.5\text{kHz}$
- (vii) For a good reference spur rejection performance, it is best to place the additional pole as close to the crossover frequency as possible without degrading phase margin. The optimal location of the additional pole is $\omega_p = \omega_c \times (4\zeta^2) = 2\pi \times 120\text{kHz}$
- (viii) Assuming the VCO gain $K_o = 2\pi \times 300\text{MHz/V}$, the PFD-CP gain is $K_D = \omega_n^2/K_o = 4.7\text{V/rad}$.
- (ix) Assuming the charge-pump current $I = 30\mu\text{A}$, the rest of the circuit elements can be calculated as follows:
 - $C_1 = I/(2\pi K_D N) = 420\text{pF}$
 - $R_1 = 1/(\omega_z C_1) = 50.5\text{k}\Omega$
 - $C_2 = 1/(\omega_p R) = 26.3\text{pF}$

5. Recent Progress in Frequency Synthesizer Design Techniques

Even though frequency synthesizer theory is very mature, there is still a large research effort aimed to improve performance and optimize implementations for new technologies and emerging standards. One of the main drivers for research in frequency synthesizers has been the need to generate increasingly higher frequencies while decreasing power consumption. This section presents a brief review of recent advances in frequency synthesizer design.

5.1. Novel Architectures

The frequency synthesizer architecture is generally based on a phase-locked loop. Dual loop architectures have been presented trying to alleviate the trade-off between loop bandwidth and frequency steps in integer synthesizers.^{17,18} An area and power consumption penalty is paid for the relaxed trade-off. A nested architecture is proposed to obtain a wide-band PLL while maintaining fine frequency resolution and spurs rejection.¹⁹ A stabilization technique introduces a zero in the open-loop

transfer function through the use of a discrete-time delay cell and relaxes the trade-off between the settling speed and the magnitude of output sidebands.²⁰

5.2. *Linearization Techniques*

In an effort to reduce spurious tones, a new topology uses charge-pump averaging and reduces the magnitude of the fractional spurs to levels below the noise floor.²¹ A DAC controlled a phase noise cancellation and charge pump linearization technique is introduced.²² Another option for charge pump linearization is to add a replica charge pump and a bias controller to compensate the current mismatch in the charge pump.²³ This technique allowed a reduction of 8.6 dB of the spurious tones.

5.3. *Digital Phase-Locked Loop*

With the improvement of digital CMOS processes, there has been an increased interest in all-digital RF frequency synthesizers.^{24,25,26} One of the main advantages of all-digital frequency synthesizers is the elimination of the PFD - charge pump non linearity, the easy integration in modern technologies and a reduced dependence on process variations. A digital PLL with a DAC to control the VCO voltage and a digital phase-frequency detector (DPFD) accompanied by an adaptive loop control helps to obtain fast acquisition.²⁴ This frequency synthesizer is mainly oriented to clock generation.

5.4. *Fast Settling Techniques*

Fast settling techniques try to relax the trade-off between settling time and loop bandwidth by providing additional means to speed the frequency switching process. A switchable-capacitor array that tunes the output frequency, and a dual loop filter operating in the capacitance domain are proposed.²⁷ A settling time smaller than 100 μs is obtained. A locking time as short as 30 μs is reported, which uses a discrete-time loop filter with a stabilization zero created in the discrete-time.²⁸ A different technique is reported where 64 identical charge pumps are enabled and the loop resistor is reduced by 8 \times , effectively increasing the loop bandwidth by 8 \times only during the switching of the synthesizer. A settling time of 10 μs is reported.²⁹

5.5. *VCO*

RF oscillator design is challenging due to the uncertainty in the modelling of its passive devices. Hence, it is the building block that has received more attention in the last few years. A phase noise of -139 dBc/Hz at 3 MHz offset is reported using a low inductor quality factor (Q) of 6 for an oscillation frequency of 1.8 GHz in a noise shifting differential Colpitts VCO.³⁰ -139 dBc/Hz at 3 MHz offset at 1.7 GHz is achieved by adding a voltage regulator to the VCO and thus reducing its sensitivity to the supply noise.³¹ A 36 GHz VCO,³² 60 GHz and 100 GHz VCOs in 90 nm technology,³³ and a 63 GHz VCO in standard 0.25 μm CMOS technology³⁴

are reported. Circular-geometry oscillators based in slab inductors,³⁵ and a circular standing wave oscillator³⁶ are presented. A stable fine-tuning loop is combined with an unstable coarse-tuning loop in parallel, and as a result, a stable PLL with a relatively wide tuning range of 600 MHz for a 4.3 GHz oscillator is obtained,³⁷ and a 20 GHz VCO with 25% tuning range achieved through the small parasitic capacitance of a negative-resistance cell.³⁸ A single loop horseshoe inductor with a quality factor larger than 20 and an accumulation MOS varactor with C_{\max}/C_{\min} ratio of 6 provide a 58.7% tuning range between 3 and 5.6 GHz.³⁹ Finally, the first digitally controlled oscillator (DCO) incorporating dithering to increase the frequency resolution of the DCO is introduced.⁴⁰

5.6. Quadrature Generation

Quadrature generation is an important part of the signal processing in an RF front-end. Most of the modern communication standards use phase or frequency modulation schemes, which require quadrature mixing to extract the information contained in both sides of the spectra.⁶

The most widely used technique involves the use of passive polyphase networks conformed of integrated resistors and capacitors. To improve the accuracy of the 90° phase shift, the order of the phase shift network has to be increased to spread the absolute value of the passive components. Phase errors as low as 3° can be obtained due to process variations of the passive elements.^{41,42,43} A drawback of this technique is that the higher the order of the polyphase network, the larger the insertion loss of the LO signal – 3 dB of attenuation per stage. Another common technique for quadrature signal generation is the use of a VCO signal generated at twice the desired LO frequency. This technique provides a broadband range of quadrature outputs, but increases the power consumption by 20 to 30% due to higher operating frequencies. The accuracy of the phase generation is limited by the matching of the flip-flops in the frequency divider and the duty cycle error of the VCO output.⁴⁴

Calibration techniques are also found in the literature; they measure the phase imbalance of the quadrature outputs and compensate it. A delay locked loop (DLL) is used to adjust the phase error in a quadrature generator.⁴⁵ A phase detector controls the current in the phase shifter and adjusts the phase different between two split paths. The duty cycle of the clock signal is changed to compensate for the phase imbalance at the output of the divide-by-two circuit by adding a DC level component to the flip-flop clock.^{46,47} A self-calibration loop tunes each branch of the phase shifter sequentially to average the phase error generated due to mismatches in the passive components.⁴⁸

5.7. Prescaler

Being one of the most power hungry blocks in the synthesizer, along with the VCO, a lot of effort has been placed into reducing its power consumption. Dynamic-logic

frequency dividers based on true-single-phase-clock (TSPC) latches have shown a low power and high speed operation.⁴⁹ Exploiting dynamic loading, an 1 V 2.5 mW divide-by-two flip-flop operating up to 5.2 GHz in 0.35 μm CMOS technology is achieved.⁵⁰ A very low power divider is based on a quasi-differential locking divider operating up to 4.3 GHz while consuming 44 μW from a 0.7 V power supply in a 0.35 μm CMOS process.⁵¹ Another approach to improve power consumption is to use the injection-locked oscillator as a frequency divider.⁵² It is shown that the injection-locked frequency divider can provide a high speed divide-by-two circuit with substantially lower power consumption than its digital counterparts.

As can be seen from the previous list of highlighted papers, there are open problems in almost every major building block of the frequency synthesizer. In particular, new architectures that allow to relax the bandwidth and settling time trade-offs, and optimization of VCO performance, along with power efficient frequency dividers, are areas for research focus.

6. Conclusion

A description of frequency synthesizers that emphasizes the key design parameters and specifications for their use in wireless applications has been presented. The mapping between the communication standard into particular specifications has been highlighted for parameters such as phase noise, settling time, and spurious rejection. A discussion on stability limits has been presented to establish the limits on the ratio of loop bandwidth with respect to the reference frequency and the relative location of the poles, zero and crossover frequency. The main design trade-offs between noise, bandwidth and stability have been described, as well as the implications on settling time and stability of the relative location of the pole and zero on the transfer function. A brief survey of the latest advances on the design of frequency synthesizers helps to identify the areas where most of the design effort needs to be put to improve the performance of the circuit. As advances in technology allow for faster and smaller transistors, the trade-offs in the design of frequency synthesizers need to be studied and exploited in the never ending search for a compact and low power transceiver implementation.

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