A GSM LNA Using Mutual-Coupled Degeneration

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***Abstract*—This letter presents a low noise amplifier (LNA) input impedance matching technique using mutual coupled inductors. This scheme not only provides the required input impedance matching but also interstage impedance transformation for the cascoded transistor. The mutual coupled inductors also help to improve the circuit's reverse isolation. A 900-MHz global system for mobile communication LNA using this technique is designed and fabricated using 0.35-μm standard complementary metal oxide semiconductor technology. It achieves a 17-dB gain, 3.4-dB noise figure, and −5.1-dBm IIP3. The LNA draws 5.6 mA from a single 2.3-V power supply.**

***Index Terms*—Input impedance matching, low noise amplifier (LNA), mutual coupling.**

I. INTRODUCTION

THE inductive source-degenerated low noise amplifier (LNA) is a very popular architecture in the integrated complementary metal oxide semiconductor (CMOS) radio frequency (RF) and microwave circuit designs [1]. It nicely trade-offs among input matching, noise figure, and gain specifications. A cascoded structure is usually used in the LNA to reduce Miller effect on input impedance and improve reverse isolation. An interstage inductor is employed in [2] and [3] to provide interstage matching. Coupled inductors (transformers) are used in [4] to provide feedback. In this letter, the mutual coupling between the degeneration and interstage inductors is added to obtain another degree of freedom for the design. Section II explains the proposed method. Detailed analysis including the input impedance, interstage impedance, and noise performance are provided. The measurement results for the proposed LNA working in the 900-MHz global system for mobile communication (GSM) band using the mutual-coupled degeneration technique is given in Section III to validate the proposed idea. Conclusions are drawn in Section IV.

II. PRINCIPLE OF IMPEDANCE MATCHING USING MUTUAL INDUCTANCE

A. Input Impedance Matching

The idea of using mutual coupled inductors in the LNA input matching network is illustrated in Fig. 1. It can be shown that the input impedance can be expressed as

$$Z_{\text{in}} = s(L_G + L_S) + \frac{1}{sC_{GS1}} + \frac{g_{m1}}{C_{GS1}}(L_S \pm M) \quad (1)$$

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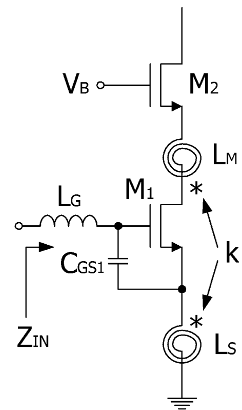

Fig. 1. Matching utilizing mutual inductance with a coupling factor $k = M/\sqrt{L_M L_S}$.

where M is the mutual inductance between L_S and L_M. Its polarity is determined by how the magnetic coupling is constructed.

For the mutual coupling polarity indicated in Fig. 1 by the asterisk, minus sign will be assigned to the third term in (1). This impedance expression resembles the one without mutual inductance coupling except that the real part is modified by the mutual inductance. Under resonant frequency condition

$$\omega_o = \frac{1}{\sqrt{(L_G + L_S)C_{GS1}}} \quad (2)$$

Z_{in} only presents resistance and no reactive part

$$R_{\text{in}} = \omega_T(L_S \pm M) \quad (3)$$

where $\omega_T = g_{m1}/C_{GS1}$. For the long channel device approximation

$$\omega_T \propto \frac{1}{L^2}\mu(V_{GS1} - V_{th1}). \quad (4)$$

The device minimum channel length L is usually chosen for high frequency performance. C_{GS1} is calculated from the optimum input quality factor $Q_I = 1/\omega_o C_{GS1} R_s$. Therefore, the device width W is obtained by solving $C_{GS1} = (2/3)WLC_{ox}$. Gate overdrive voltage $V_{GS1} - V_{th1}$ can be fixed by power consumption constraint $I_D \propto (W/L)(V_{GS1} - V_{th1})^2$ or linearity requirement $IIP3 \propto V_{GS1} - V_{th1}$.

For a conventional inductive degenerated LNA, difficulty may arise from using high bias level to obtain high input linearity. Input match condition requires $R_s = \omega_T L_S$, where R_S is usually 50 Ω or 75 Ω. For high gate bias level, $V_{GS1} - V_{th1}$ is large, therefore, ω_T is also large. This situation will probably require a very small degeneration inductance of L_S, which is hard to design or already comparable to the bond wire

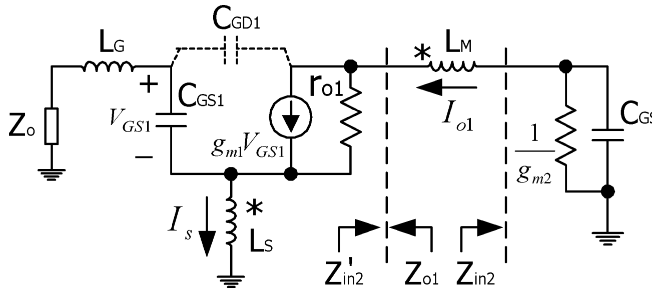

Fig. 2. Interstage impedance.

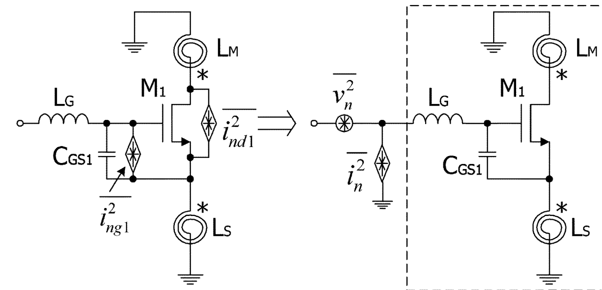

Fig. 3. Equivalent input noise sources of the inductive coupled LNA.

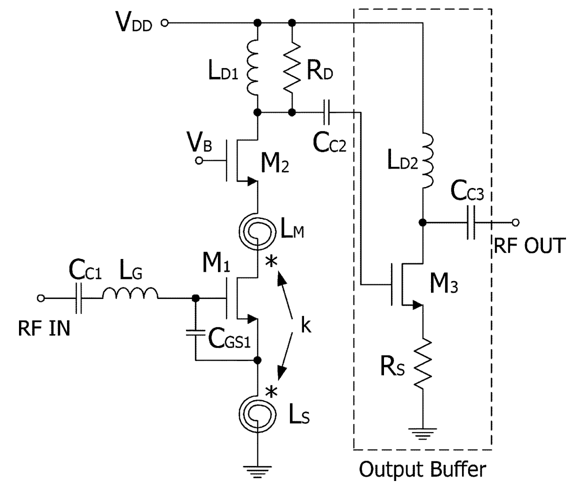

Fig. 4. Proposed mutual-coupled degenerated LNA.

inductance. Of course, bond wire can be used but it is less controllable by the designer and is affected by the placement of the die in the package which is unknown at the very beginning of the design stage. Small L_S will also require large L_G to provide the same resonant frequency ω_o, while large inductances generally have a larger series resistance which will degrade the noise figure of the LNA, because L_G is directly in series with the gate. However, the presence of the mutual inductance offers another degree of freedom for input impedance matching. By choosing the negative sign in (1), $R_s = \omega_T(L_S - M)$, larger L_S can be used. If the design is targeting on minimum current consumption, and if $V_{GS1} - V_{th1}$ is small, a large L_S may be required. In this case, a positive sign in (1) can be used to enable smaller degeneration inductance.

B. Interstage Impedance

In Fig. 1, cascoded transistor M_2 reduces Miller effect and provides output–input isolation. Adding L_M can provide interstage impedance transformation and help to further reduce Miller capacitance of M_1, therefore, increasing reverse isolation. Fig. 2 shows the small signal equivalent circuit for interstage impedance calculation. Z_o is the source impedance. $1/g_{m2}$ in parallel with C_{GS2} represents the input impedance of cascoded stage. Intuitively, the common-gate configured transistor M_2 has an input resistance of about $1/g_{m2}$ (actually it is larger than $1/g_{m2}$ because the drain of M_2 is not shorted to ac ground. $1/g_{m2}$ is a good approximation for low-load impedance though). The M_2's gate-source capacitance C_{GS2} together with inductor L_M form a shunt-series impedance transformation network. This network transforms $1/g_{m2}$ to a smaller value.

The impedance looking into the drain of M_1 is

$$Z_{o1} = 2r_{o1} + \frac{\omega_o^2}{\omega_T}L_s + j\frac{\omega_o}{\omega_T}Z_o. \tag{5}$$

Usually, ω_o is far below ω_T and Z_o is 50 or 75 Ω, so the reactive part of (5) will be relatively much smaller than the resistive part. Z_{o1} will be nearly resistive. Note that C_{GD1} will mainly affect Z_{o1}. However, Z_{o1} is high, therefore we ignored C_{GD1} for our impedance analyses. Looking away from the drain of M_1, the impedance can be shown to be

$$Z'_{in2} = \frac{1}{g_{m2}}\frac{1}{1+\left(\frac{\omega_o}{\omega_{T2}}\right)^2} \pm \left(\frac{\omega_o}{\omega_T}\right)^2 \omega_T M + j\omega_o\left[(L_M \pm M) - \frac{1}{g_{m2}}\frac{\omega_{T2}}{\omega_{T2}^2+\omega_o^2}\right] \tag{6}$$

where $\omega_{T2} = g_{m2}/C_{GS2}$. By choosing proper ω_{T2}, Z'_{in2} can have only a resistive part and its value is smaller than $1/g_{m2}$. The effect is that there will be more current pumped into the cascoded stage thus improving efficiency. The voltage gain from the gate of M_1 to its drain terminal will be decreased due to a reduced load impedance, thus reducing Miller feedback effect. The reduced voltage gain also leads to a smaller signal swing at the drain of M_1, so the signal fed back to the input is reduced.

C. Noise Performance

In an LNA with the cascoded structure, the cascoded MOS transistor has little effect on the noise performance [5] of the whole circuit, its noise contribution will be ignored in the following noise analysis. M_1's drain noise current $\overline{i_{nd1}^2}$ and induced gate noise current $\overline{i_{ng1}^2}$ will be represented by a noise voltage $\overline{v_n^2}$ and noise current $\overline{i_n^2}$ as shown in Fig. 3. It can be shown that at around operation frequency ω_o

$$\overline{i_n^2} = \overline{\left(i_{ng1} + i_{nd1}j\frac{\omega_o}{\omega_T}\right)^2} \tag{7}$$

and

$$\overline{v_n^2} = \overline{\left(-\frac{i_{ng1}}{j\omega_o C_{gs1}}\right)^2}. \tag{8}$$

Since the mutual inductance does not appear explicitly in the above equations, it does not make the expression forms of input

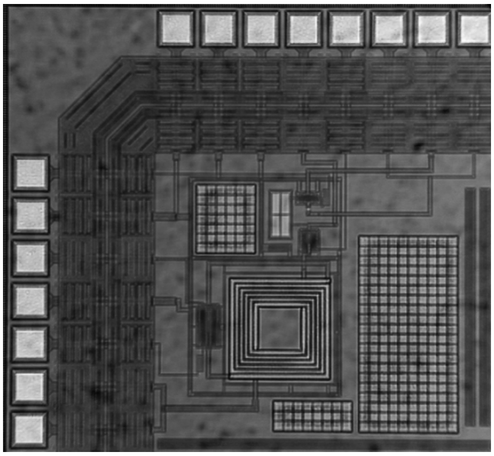

Fig. 5. Die microphotograph of the proposed LNA.

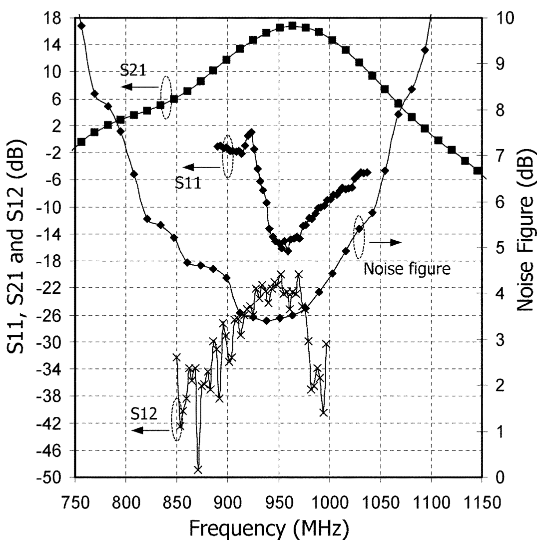

Fig. 6. Measure small signal performance the proposed LNA.

equivalent noise sources different from a regular inductive degenerated LNA [1].

III. Chip Measurement Results of the Mutual-Coupled Degenerated LNA

A mutual-coupled degenerated LNA is implemented using TSMC 0.35 μm CMOS technology. Fig. 4 is the schematic of the proposed LNA, and the die micro-photograph is shown in Fig. 5. The mutual coupled inductors L_M and L_s are implemented on-chip by two interleaved square spirals. The inductor L_G is formed by the bond wire and off-chip surface mount inductor. Multiple bond pads are used for ground connections to reduce the ground inductance. The LNA occupies 700 μm $\times$ 500 μm active silicon area.

Fig. 6 shows the measured small signal performance of the proposed LNA. The gain (S21) is 17 dB at 950 MHz. The total noise figure is 3.4 dB which is higher for GSM application. However, this is because it includes the output buffer formed by M_3, R_s, and L_{D2}. Bonding pads and inferior quality factors of inductors also makes the NF larger. Simulation shows that the LNA, with better inductors and bonding pads removed, has a noise figure about 1.4 dB. The LNA is tested within a plastic package and soldered on a PCB. The measured IIP3 plot is illustrated in Fig. 7, which is -5.1 dBm. The LNA draws 5.6 mA from a single 2.3-V power supply. Table I summarizes the measurement results of the proposed GSM LNA.

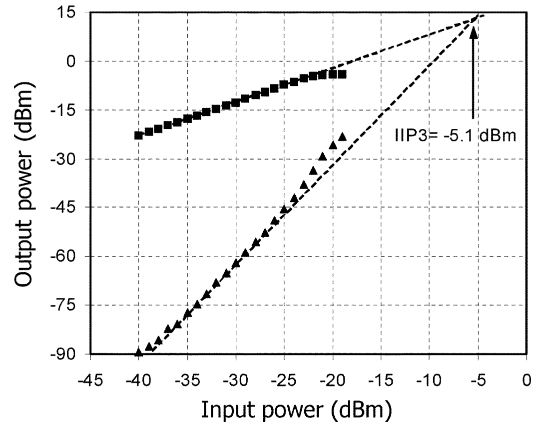

Fig. 7. Measured IIP3 of the mutual-coupled degenerated LNA.

TABLE I
PERFORMANCE OF THE PROPOSED LNA AT 950 MHz

Parameters	Value	Unit
Gain	17	dB
NF	3.4	dB
S11	-14	dB
S12	-22	dB
IIP3	-5.1	dBm
Power	13	mW

IV. Conclusion

A 900-MHz GSM LNA using the proposed mutual-coupled source degeneration was designed, fabricated, and fully characterized. It achieved 17-dB gain, 3.4-dB noise figure, and -5.1-dBm IIP3. The LNA draws 5.6 mA from a 2.3-V power supply. By introducing coupling between the source degeneration inductors and interstage inductors, another degree of freedom is obtained for the LNA design. The proposed scheme not only provides input impedance matching but also improves reverse isolation $(S12 < -22$ dB$)$.

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