



A 270 MHz, 1 V_{pk-pk}, Low-Distortion Variable Gain Amplifier in a 0.35 μm CMOS Process

SIANG TONG TAN* AND JOSÉ SILVA-MARTÍNEZ

Analog and Mixed Signal Center of the Department of Electrical Engineering, Texas A&M University, College Station, Texas, USA
E-mail: sttan@ti.com; jsilva@ee.tamu.edu

Received June 15, 2002; Revised January 7, 2003; Accepted February 14, 2003

Abstract. A fully balanced CMOS Variable Gain Amplifier (VGA) based on current-mode techniques suitable for high frequency applications and large signals is presented. The VGA consists of an analog multiplier, current gain stages, and resistive loads. A frequency compensation scheme based on a capacitive feed-forward technique increases the bandwidth by more than 60%. Common-Mode Feed-Forward (CMFF) techniques are used to minimize dc offsets. The gain can be programmed from 0 to 42 dB with -3 dB bandwidth greater than 270 MHz; a gain calibration scheme for precise gain control applications is included. The Third Harmonic Distortion (HD3) is less than -55 dB for differential input and output voltages of 1 V_{pk-pk}. The VGA was fabricated in a standard 0.35 μm CMOS process, and consumes around 54 mW from a single power supply of 2.7 V.

Key Words: variable gain amplifiers, current-mode circuits, current mirrors, analog multipliers, frequency compensation, common-mode feed-forward, low power

1. Introduction

A VGA adjusts the amplitude of the incoming signals to a level that can provide the largest signal-to-noise ratio for the next stage; hence the dynamic range of the overall system improves. If the input signals of a system are unpredictable, an Automatic Gain Control (AGC) based on a VGA is used to fix the output signals to the optimal level. The VGA's bandwidth and linearity requirements are higher than those of following stages, otherwise the overall performance of the system is degraded. VGA noise figure is another important concern if the input signals are very small. Also, several applications require very wide variable gain range; therefore gain steps in logarithm scale are commonly used.

The selection of the VGA architecture depends on the given specifications; for this design, we are mainly interested in achieving high bandwidth and handling signals up to 1 V_{pk-pk}. The most popular open-loop VGA architectures are based on source degeneration techniques [1, 2], analog multipliers [3] and differential pairs with diode-connected loads [4, 5].

The voltage gain of source degeneration circuits depends on load and source resistors; for large amplification factors large load resistors are required, limiting the amplifier's bandwidth. The source resistance can be reduced to alleviate this drawback, but larger input transistors are required in order to increase the degeneration factor. Transconductance boosting circuits, which might limit the bandwidth and cause stability issues, are normally used to enhance the transconductance of the input drivers [1]. The analog multiplier provides good linearity and fast response. Although large variable range might be achieved by using a single multiplier, there are several design tradeoffs involved. If huge variable gain is used, the input referred noise increases further for minimum gain settings. On top of that, a logarithmic gain control circuit is needed to provide gain steps in dB scale [3]. The differential pair with diode-connected loads is based on voltage amplifiers. These topologies are based on non-linear V-I and I-V conversions, and are partially linearized if proper bias currents are used. Since this structure is based on the operation of two differential pairs, the amplitude of the signals must be not larger than $V_{GS} - V_T$, otherwise the differential pair does not operate properly. The voltage

*Present address: Texas Instruments, Dallas, USA.

gain depends on input-output bias currents and transistor aspect ratios. Typically, the previously discussed structures require a common-mode feedback circuitry per stage. Other techniques using simple differential pairs [6] and pseudo differential pairs [7] have also been reported. Although high bandwidth and large input drivers' transconductance can be achieved, it can only handle moderate or small input signals. All these architectures are based on voltage amplification, and they are not very well situated for VGA applications where supply voltages are limited and large high-frequency signals have to be driven.

In this paper, a VGA based on the combination of a four-quadrant multiplier and current gain stages is employed. The VGA can operate from DC up to 270 MHz for input and output signals of $1 V_{\text{pk-pk}}$ while HD3 is less than -55 dB. Adding frequency compensation circuits increases the VGA bandwidth by more than 60%. Common-mode feed-forward stages strategically located reduce common-mode offsets. Since the current gain is digitally controlled in steps of 6 dB, special magnitude control for logarithmic scales is not required. An additional fine-tuning control is used for the adjustment of the multiplier's gain. The VGA architecture is described in Section 2; Section 3 deals with the design issues of the building blocks. Guidelines for high-frequency and low-distortion system design are provided. The experimental results are given in Section 4; some conclusions are addressed in the last section.

2. VGA Architecture

MOS devices have limited small signal transconductance; hence it is challenging to achieve high gain and high frequency at the same time. In general, the voltage gain for a single amplifier is given by $g_m R_L$, where g_m is the small signal transistor's transconductance and R_L is the load resistance. The load resistance is limited by the bandwidth requirements, and g_m for a single MOS device, in $0.35 \mu\text{m}$ processes, is normally less than 10 mS due to power and silicon area limitations. A common design approach is cascading several amplifiers. For voltage amplifiers the input signal is usually small, and the amplifiers are tailored according to the signal level. This approach cannot be used here because for small VGA gain factors the signal swing is large for all stages; as a result, all stages have to be able to handle large signals. This drawback might be overcome if analog switches are used to bypass some sections; due to the large swing of the signals the switches introduce additional distortion and switch resistance limits its frequency response.

Current-mode circuits can be used for the amplification of high frequency signals. The input voltage can be converted into current by a linear OTA, and the signals are amplified using current mirrors; the basic architecture is shown in Fig. 1.

The current is amplified by scaling the transistor dimensions and bias currents. The overall voltage

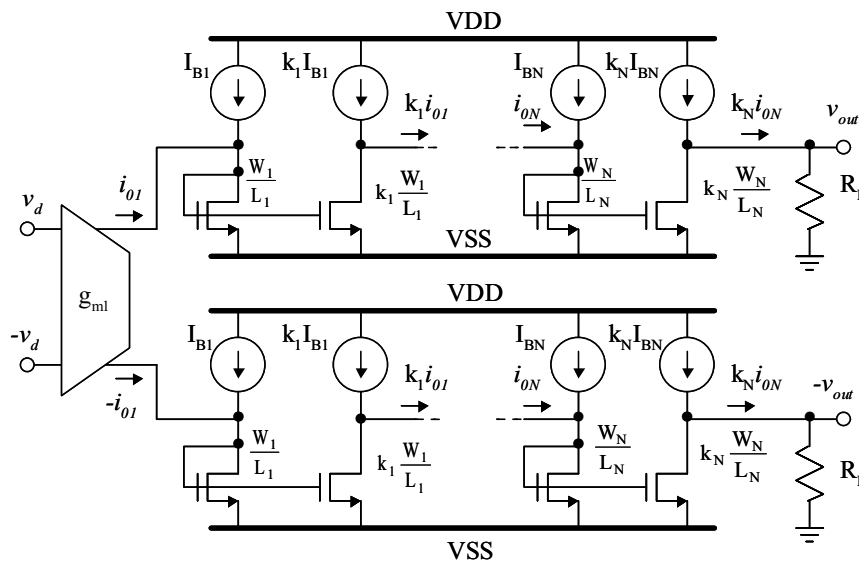


Fig. 1. Variable gain amplifier based on current mode.

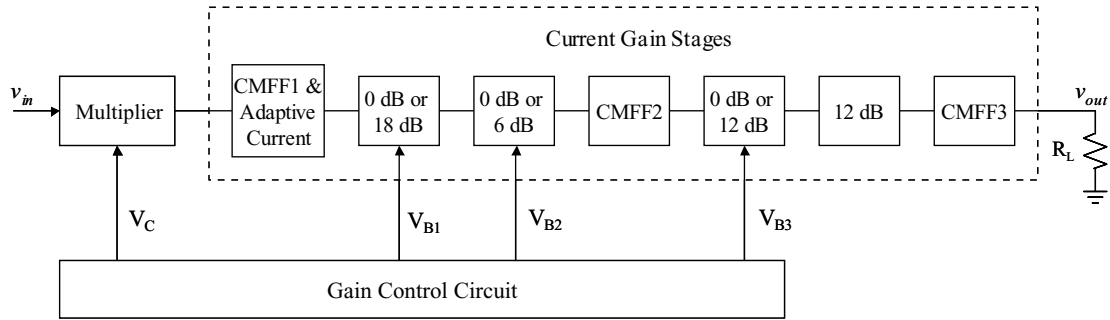


Fig. 2. Block diagram of the proposed VGA.

gain is

$$\frac{v_{out}}{v_d} = g_m[k_1 k_2 \dots k_N] R_L \quad (1)$$

where k_j is the current gain of the j th current mirror stage. The current mirrors are used for coarse control with gain steps of 6 dB or more, and the fine control is carried out in the OTA. An advantage of this circuit is that all internal nodes are low impedance, hence the structure can operate at high frequencies. Since the signals are currents, the voltage swing in the internal nodes is small; therefore this topology is suitable for low-voltage applications. Besides, no common-mode feedback is required because the diode-connected transistors fix the common-mode voltages.

The VGA building blocks and gain distribution are shown in Fig. 2. An analog multiplier is used as a transconductor because it can handle large signals and provides enough linear range. The gain control system consists of the 6 dB fine-tuning section that adjusts the multiplier's transconductance g_m to provide gain steps of 1 dB or even less if required. Besides, linear-to-exponential circuitry [3] is not needed because the required multiplier variable gain range is small. The control circuit drives several current switches to select the current gain factor of 6, 12 and 18 dB in order to provide variable gain range of 0–36 dB in 6 dB steps. All current gain blocks are realized by cascading current mirrors with 6 dB gain each.

The multiplier output current is injected into a block that provides a current gain of 0 or 18 dB. Since the bias current of the multiplier changes with the control voltage, an adaptive current sink and a Common-Mode Feed-Forward (CMFF) stage, to be discussed in the next section, are used to cancel the offset currents. After this block, current gain stages providing 0–6 dB

and 0–12 dB current gain, respectively, are included. Additional CMFF stages remove common-mode current offsets. In order to boost the output current to the desired level, another stage providing 12 dB gain is included; as a result of the use of this current stage, the current consumption of the previous stages is reduced. The benefits of using this stage are twofold: firstly, both current swing and current consumption reduce and secondly, the noise is minimized. For current-mode circuits, the important parameter to be optimized is the current noise density, which increases with the bias current. The limit for the bias current is determined by harmonic distortion and speed constraints.

3. Description of the Main Building Blocks

The schematic of the analog multiplier is shown in Fig. 3 [8]. All transistors operate in saturation region, resulting in very high frequency response. V_X and V_Y are the common-mode levels for the differential input signals, v_x , and the control voltages, v_y , respectively.

Since all transistors have to operate in the saturation region, the following bias conditions must be satisfied,

$$\begin{aligned} V_Y - v_y &> V_X + v_x + V_T \\ V_X - v_x + V_T &> v_a, v_b \end{aligned} \quad (2)$$

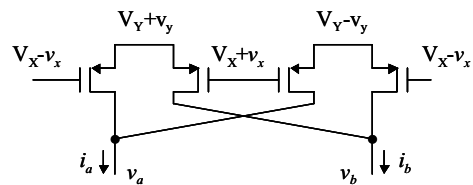


Fig. 3. The analog multiplier.

where V_T is the threshold voltage of the PMOS transistors, v_a and v_b are the multiplier's output voltages, which are set by the first current mirror (see Fig. 1). The multiplier transconductance is given by,

$$g_m = \frac{i_{out}}{v_{id}} = 2K_P \frac{W}{L} v_y \quad (3)$$

where $i_{out} = i_a - i_b$, $v_{id} = 2v_x$, and K_P is the transconductance gain of the PMOS transistors. The multiplier's transconductance is adjusted by varying the control voltage v_y ; if required, additional tuning circuitry can be used to improve its absolute value. Since $V_Y + v_y$ and $V_Y - v_y$ are applied to the source of the transistors, both transistor source and bulk have to be connected together to eliminate body effect, otherwise threshold voltage variations could be as large as 0.4 V, degrading the multiplier's linear range. The multiplier is designed for the largest possible transconductance in order to achieve better noise performance.

An adaptive current sink is used to eliminate the multiplier dc current. A replica of the multiplier with ac grounded inputs but driven by the control voltage is used. The offset currents of the current gain stages are accumulated and amplified by the following gain stages and eventually could saturate the last stages. A CMFF circuit is used to minimize offset currents; the schematic is shown in Fig. 4. Replicas of the incoming currents including offset components, $I_{OFF} + I_B + i_{ac}$ and $I_{OFF} + I_B - i_{ac}$, are added at node V_{CM} , and the resulting common-mode current $I_{DC}(=I_{OFF} + I_B)$ is mirrored to the current mirror output in order to can-

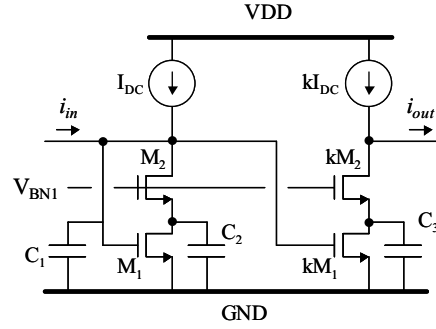


Fig. 5. Current mirror with current gain factor of k .

cel out the dc components. Therefore, next stage bias current is not longer a function of previous circuitry, and it can be properly selected according to distortion, noise and bandwidth requirements. Transistors driven by V_{BN2} and V_{BP2} are used to improve the accuracy of the circuit.

High swing current mirrors are used to provide the proper current gain; the basic building block is shown in Fig. 5. They have low input impedance and high output impedance, but moderate compliance voltage. Since the upper transistors fix the V_{DS} of the lower transistors, they are precise and little sensitive to Miller effects. Special attention must be paid to the selection of the additional bias voltage V_{BN1} to ensure that all transistors are always working in saturation region. All current mirrors were designed for the same saturation voltage ($=V_{GS} - V_T$). Designing the current mirrors with identical saturation voltage further improve the accuracy when cascading the current mirror

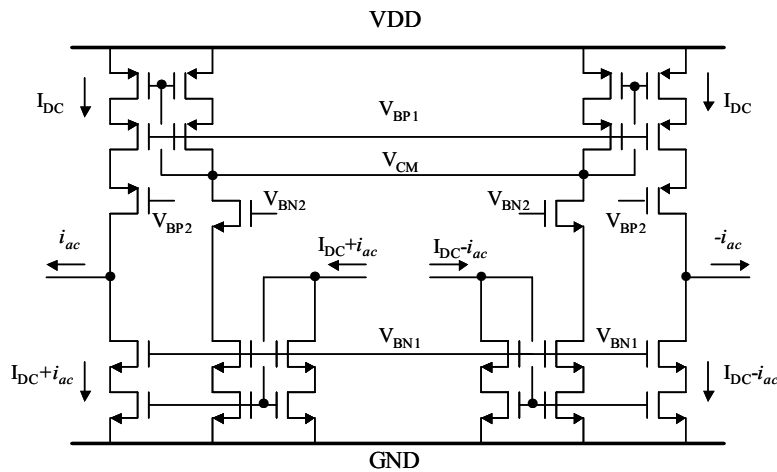


Fig. 4. High swing current mirror with common-mode feed-forward circuit for DC offset cancellation.

gain stages since the V_{DS} for both the lower and the upper transistors are similar for all stages. Also, poles of all current mirrors remain around the same frequency.

For a cascade of *m* identical current mirrors with single stage gain *k* (=2 for this design) the overall small signal current gain is given by,

$$\frac{i_{out}}{i_{in}} = \left[\frac{\frac{k g_{m1} g_{m2}}{(k+1) C_1 C_2}}{s^2 + \frac{g_{m2}}{C_2} s + \frac{g_{m1} g_{m2}}{(k+1) C_1 C_2}} \right]^m \quad (4)$$

where *C*₁ and *C*₂ are the parasitic capacitance of the lower and upper transistors, respectively; these capacitors are shown in Fig. 5. Further analysis of Eq. (4) shows that the bandwidth decreases rapidly for the first three stages, but it is relatively constant for larger number of stages. Also, in order to achieve the highest bandwidth, the gain per stage must be limited; e.g. *k* = 2, leading to current gain of 6 dB per stage. The saturation voltage, V_{DSAT}, was optimized for maximum bandwidth. Besides, bandwidth can be further improved if the quality factor of the second-order transfer function (= (g_{m1} C₂ / (g_{m2} C₁ (1 + k)))^{1/2}) is set in the range of 0.7–1.

The linearity of a current mirror is very good compared with voltage-mode amplifiers. The current mirroring is based on non-linear voltage-current and non-linear current-voltage conversions; hence both quasi-linear capacitors and quasi-linear transistor output resistance generate harmonic distortion components. It can be shown that the effects of the transistor output resistance are relatively small, but due to the presence of the parasitic capacitors (mainly due to C_{GS}) the current mirror might generate large harmonic

distortion components; HD3 is given by [9],

$$HD3(\omega) = \frac{3}{32} \left(\frac{\omega}{\omega_0} \right) \left(\frac{i_{pk}}{I_{bias}} \right)^2 \quad (5)$$

where ω₀ is the –3 dB frequency of the current mirror. *I*_{bias} and *i*_{pk} are the bias current and the amplitude of the ac current, respectively. The harmonic distortion components are function of the frequency because the impedance of the capacitor is frequency dependent. Notice that the larger the current gain factors the larger the parasitic capacitors are; therefore ω₀ reduces and the harmonic distortion components increase. For HD3 < –60 dB at ω/ω₀ = 0.1, it is required to use a bias current larger than 3 times the peak current. In this paper, the bias currents are computed according to this rule of thumb.

Frequency compensation techniques can increase the –0.5 dB bandwidth as well as the –3 dB bandwidth. In this design, a capacitive feed-forward compensation scheme is used; the basic concept is shown in Fig. 6(a). The small signal transconductance of the compensating scheme has a high pass characteristic. If for sake of simplicity g_{mc}/C_c = g_{m2}/C₂ it can be shown that the third pole of the system is cancelled by a zero, and the overall current gain of the compensated current mirror shown in Fig. 6(b) becomes

$$\frac{i_{out}}{i_{in}} = - \frac{\frac{g_{mc}}{(1+k)C_1} \left(s + \frac{k g_{m1} g_{m2}}{g_{mc} C_2} \right)}{s^2 + \frac{g_{m2}}{C_2} s + \frac{g_{m1} g_{m2}}{(1+k)C_1 C_2}} \quad (6)$$

The overall current gain consists of two poles and one zero. The additional circuit introduces current gain boosting at high frequency. Changing the tail current of

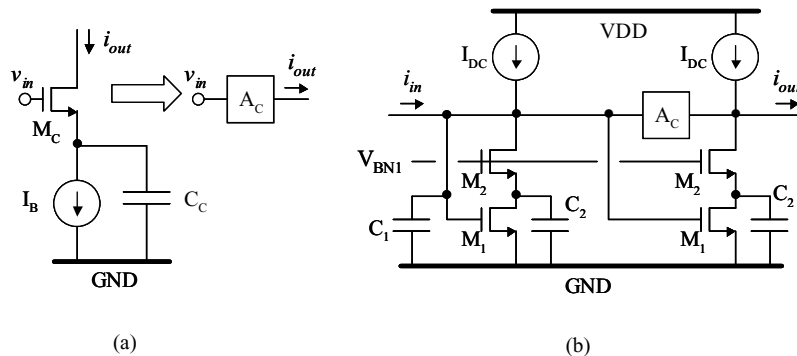


Fig. 6. Frequency compensation scheme: (a) basic single-ended circuit and (b) current mirror with compensation.

the compensating circuitry can easily control the frequency of the zero. In the actual implementation, fully-differential compensating circuits were used; compensation circuits are added to the first two CMFF stages (see Fig. 2). The required compensating capacitors are very small, around 100 fF, and the precision of these components is not a major issue.

In Fig. 2, the gain control circuit provides the selection of 6, 12 and 18 dB gain step. Figure 7(a) shows the block diagram of the 0–12 dB gain step control with two outputs. Circuit implementation of the programmable current mirror is shown in Fig. 7(b). Turning the cascode transistors ON or OFF by controlling V_{A1} , V_{B1} , V_{A2} and V_{B2} sets the current gain. Notice that no additional switches are added in the signal path. i_{out1} and i_{out2} are connected to following stages to provide the proper current gain.

For all the current gain stages, except the last one, the bias current ($=160 \mu\text{A}$) is the same because all current mirrors have to handle the same maximum current required for 0 dB gain. The bias current of the last, fixed current gain, stage is $320 \mu\text{A}$ and the bias currents for each transistors in the first, second and last CMFF blocks are 320, 160 and $640 \mu\text{A}$, respectively. Transistor dimensions are given in Table 1.

The distortion and the input referred noise limit the upper bound and lower bound of the input signal. Using conventional noise analysis techniques it can be shown that the total input referred noise power density for

Table 1. Transistor dimensions. Bias current for all transistors is $160 \mu\text{A}$.

Building block	W/L ($\mu\text{m}/\mu\text{m}$)
Multiplier	40/0.8
Current gain stages, except the last one	NMOS 10/0.4
	PMOS 16/0.4
Common-mode feed-forward, second one	NMOS 10/0.4
	PMOS 16/0.4
Frequency compensation (drivers)	16/0.4

maximum gain is given approximately by,

$$\bar{v}_{in}^2 \cong \frac{2i_{M1}^2 + 2i_{M2}^2 + 6i_C^2}{g_m^2} + \frac{6(i_N^2 + i_P^2)}{g_m^2} \quad (7)$$

where g_m is the multiplier transconductance. In this equation, i_{M1}^2 and i_{M2}^2 are the noise contribution of the transistors used in the multiplier; the noise contribution is different for these transistors because their bias current is different (a couple of these devices are connected to $V_Y + v_y$ and the other two are driven by $V_Y - v_y$). i_C^2 is the noise current density of the transistors used in the adaptive current sink. i_N^2 and i_P^2 are the noise current density of the NMOS and PMOS devices in the current mirrors, respectively. Input referred noise power due to the first current gain stage and the first CMFF are given by the second term.

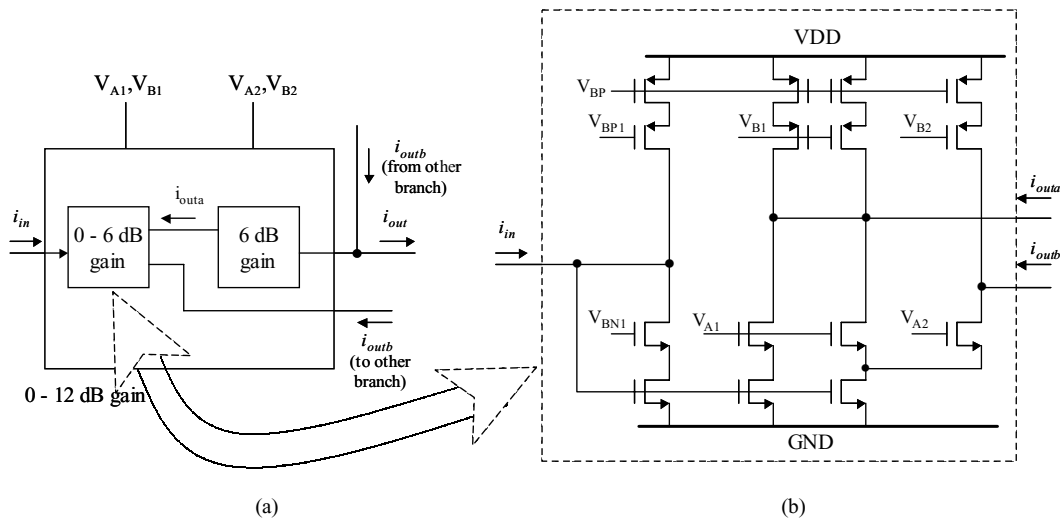


Fig. 7. Circuit implementation of the current mirror gain control for 0–12 dB gain: (a) block diagram and (b) circuit implementation of the 0–6 dB gain sub-block.

Noise contribution of other current gain stages, frequency compensation circuits and load resistors are negligible.

Equation (7) shows that the input referred noise is normally dominated by the first few stages since the output noise from each stage will be divided by the gain of it previous ones. Of course, increasing the multiplier transconductance can reduce the input referred noise. Besides, if the bias current of the current mirror is increased, the input referred noise will be increased as well because noise current density is proportional to the transconductance gain of the current mirrors and CMFF sections.

The gain step of the overall VGA is very precise. However the absolute value of the transconductance gain of the multiplier and load resistance are sensitive to variations of both process parameters and temperature; for many applications such as instrumentation applications absolute gain is also important. A simple calibration circuit operating at dc can be implemented to fulfill this requirement. The proposed scheme is shown in Fig. 8; switches and resistors control the OTAREF's transconductance; the switches are controlled by the external digital code. A replica of the multiplier and a precise linear voltage to current converter (OTA_{REF}) based on source degeneration using linear resistors are employed. The reference voltage V_R generates output current in both multiplier and OTA_{REF}. The multiplier output current, proportional to its transconductance, is compared with the OTA_{REF} output current, and the error current is used to generate the multi-

plier's control voltages $V_Y \pm v_y$. The common-mode feedback circuit provides the common-mode voltages (V_Y) for both multiplier and OTA_{REF} outputs. Under steady state condition, the overall current injected into the load capacitors is zero, leading to the condition $g_{m_multiplier} = g_{m_REF} \cong 1/R$. If required, regulated drivers can be used to improve the accuracy of OTA_{REF}. The degeneration resistors of OTA_{REF} can be matched with the VGA load resistors to provide more precise voltage gain, which should depend on the ratio of those resistors.

4. Experimental Results

The VGA has been fabricated in a standard 0.35 μm CMOS process through the MOSIS service. The chip microphotograph is shown in Fig. 9; active area for the whole VGA is 630 × 240 μm². The chip operates with a single power supply of 2.7 V, and the maximum power consumption is around 54 mW. For the chip characterization baluns and resistive matching networks were used. Therefore, the voltage gain measured is attenuated due to the small impedances (=50 Ω) connected to the VGA output.

Figure 10 shows the VGA frequency response for current gains from 4 dB up to 40 dB in steps of 6 dB. The -3 dB bandwidth is around 270 MHz. For these results, the drain current of the frequency compensating circuit was set to 10 μA only. In-band gain errors are well below 1 dB for all settings. The worst case for

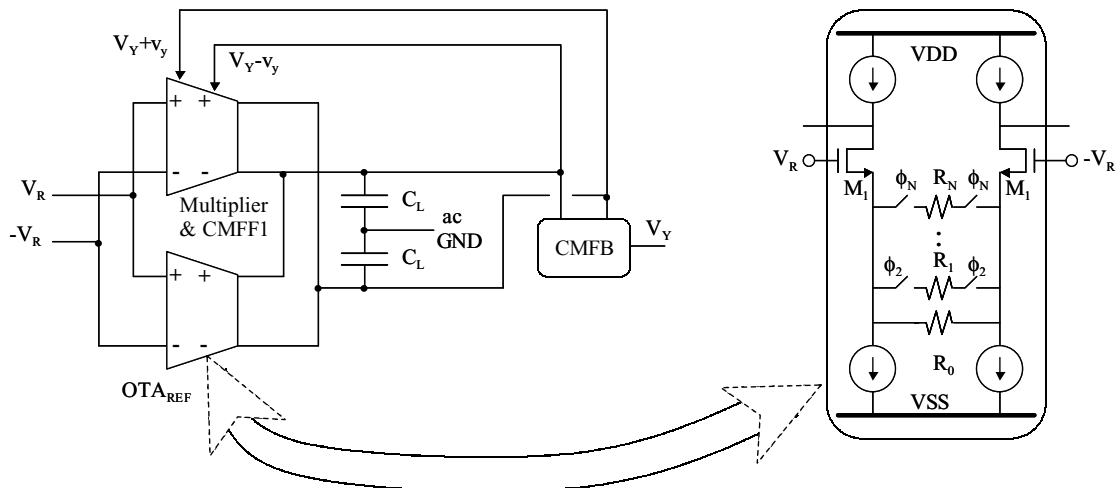


Fig. 8. Block diagram of the multiplier's tuning scheme.

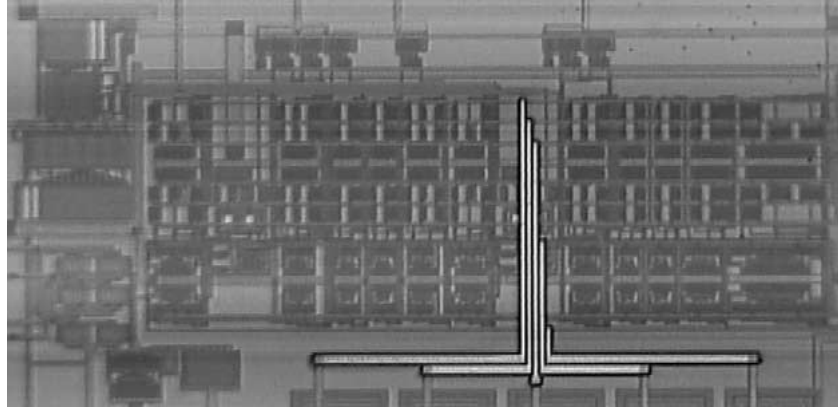


Fig. 9. Microphotograph of the chip.

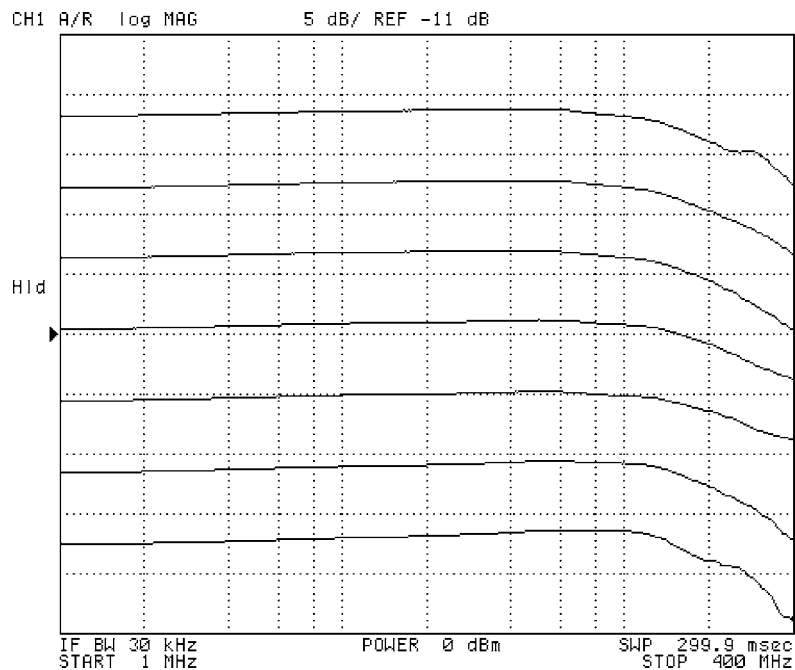


Fig. 10. Experimental frequency response of the VGA for several gain settings.

harmonic distortion occurs for 0 dB gain setting since signal level is large for all stages; under this setting, HD3 is below -55 dB for $1 V_{pk-pk}$ differential input voltage. The second and third harmonic distortion components are shown in Fig. 11. It was experimentally found that the second harmonic distortion is mainly due to the signal generator, converted into differential signal by the balun.

The frequency compensating scheme was experimentally characterized as well. The -3 dB frequency

can be increased from 270 up to 370 MHz, as shown in Fig. 12. For these results, the bias current of the compensating scheme was 6, 20 and $60 \mu A$. It can be seen from these results that the larger the compensation the larger the peaking effects are. It was experimentally found that the bandwidth can be extended by 60% without severe peaking; these results are in good agreement with the expected improvement.

In Fig. 13, the differential gain is compared with the common-mode gain for maximum gain setting. The

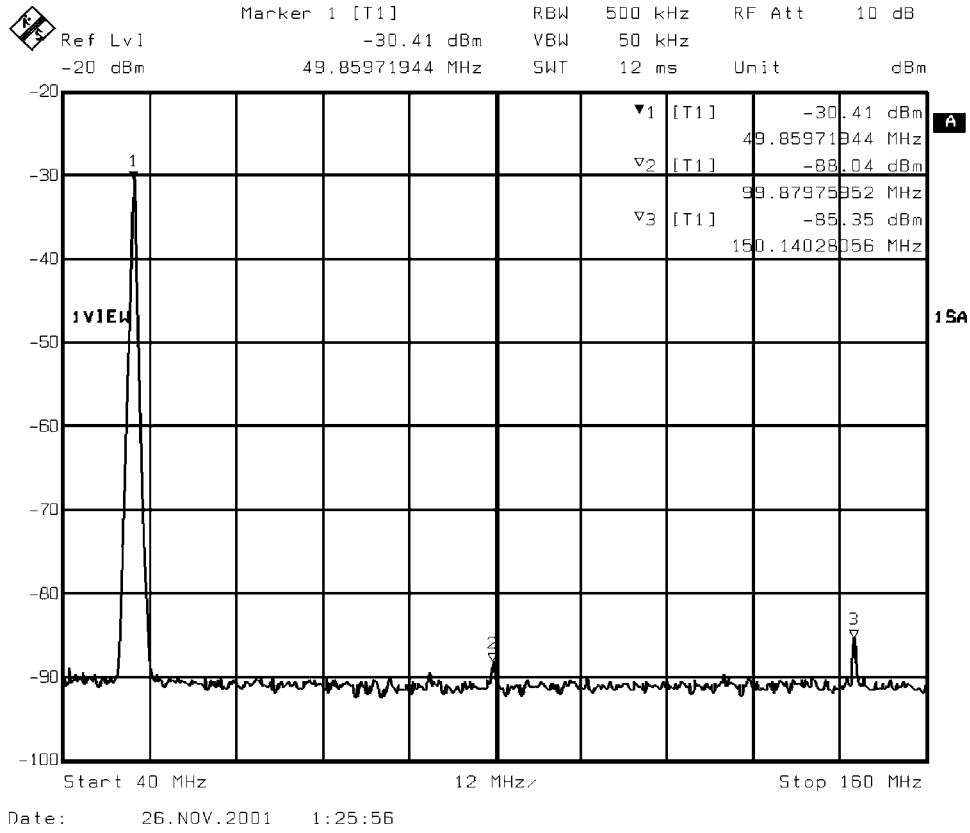


Fig. 11. Experimental results: fundamental, 2nd and 3rd harmonic of the output signal for 0 dB gain setting.

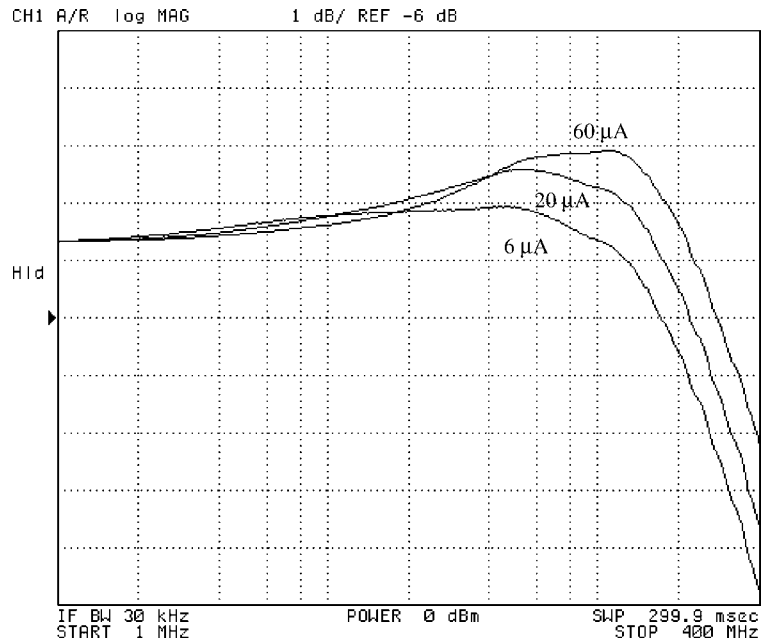


Fig. 12. Effects of the frequency compensation scheme. The bias current is 6, 20 and 60 μ A.

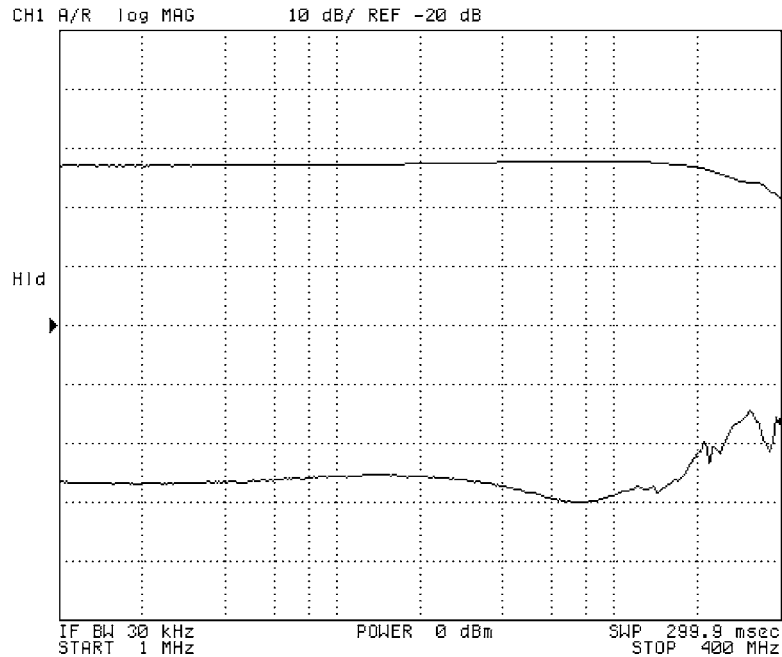


Fig. 13. Differential gain (top trace) and single output response for common-mode input signal (lower trace) for maximum gain setting.

common-mode gain transfer function (bottom trace) is obtained by applying a common-mode input signal and measuring one of the outputs. It can be seen that the common-mode rejection ratio is more than 50 dB for maximum gain setting. The VSS power supply rejection ratio (the most critical one) at 200 MHz is better than 40 dB for all voltage gain settings. The experimental results for differential gain and negative supply gain for minimum gain settings are shown in Fig. 14. The input referred noise level, integrated over the 300 MHz

bandwidth, is around 500 μV for a voltage gain of 40 dB.

A comparison of recently reported architectures is shown in Table 2. Besides technology, maximum gain greatly affects the VGA bandwidth. Cascading two identical VGA, the bandwidth will approximately decreased by half, therefore a figure of merit for a cascaded VGA can be defined as,

$$F_{\text{GBW}} = \text{Gain(dB)} \times \text{Bandwidth} \quad (8)$$

Table 2. Comparison of previously reported structures and the proposed one.

Ref.	Technology (μm)	Band-width (MHz)	Gain range (dB)	Power (mW)	Power supply (V)	Gain, V_{in} and V_{out} @ HD3 = -55 dB			F_{GBW}
						Gain (dB)	V_{in} (mV _{pp})	V_{out} (mV _{pp})	
[4]	0.4	71 (-2 dB)	-17-54	6	3	Max	0.18	99	3877
[6]	0.35	200	-45-45	35.6	3.3	Max	1.47	261	9000
						Min	147	0.82	
[7]	0.25	210	-35-55	27.5	2.5	Max	1.4	787	11550
						Min	56	0.99	
[10]	0.25	100	5.8-17	6.75	2.5	Min	718*	1400*	1700
This work	0.35	270	0-42	54	2.7	Min	1000	1000	11340

*These results are for HD3 < -80 dB.

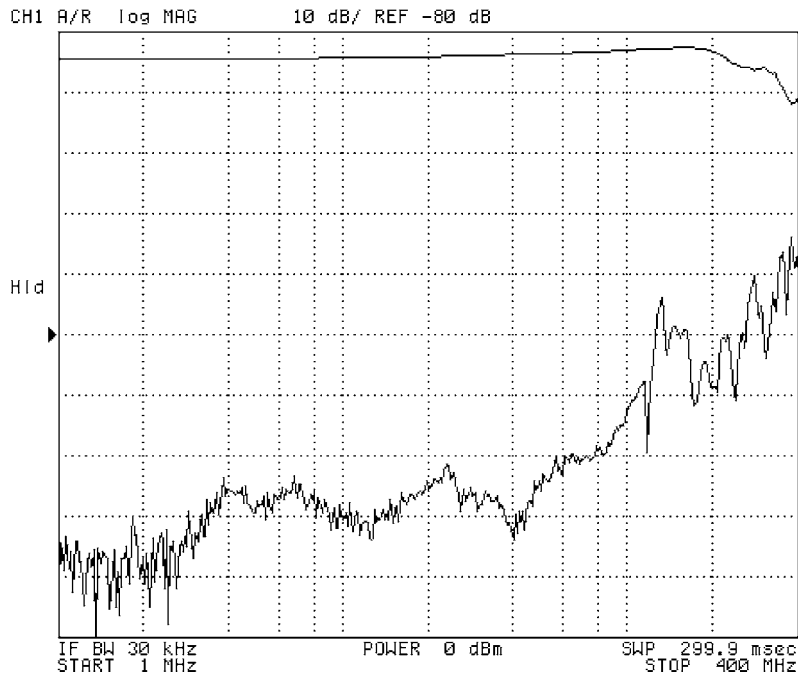


Fig. 14. Differential gain (top trace) and single output negative supply gain (lower trace) for minimum gain setting.

For linearity, other distortion descriptions such as 1-dB compression point and IIP3 in other papers were roughly converted into $HD3 = -55$ dB. A figure of merit for the VGA linearity is, for a given harmonic distortion, the sum of the VGA output and input voltage for maximum and minimum gain setting, respectively.

The F_{GBW} of the VGAs in [6, 7] are comparable with this work. However, the input stage of these VGAs cannot handle large signals due to their simple input stage. Although the topology reported in [10] presents extremely good linearity, that topology uses a regulated loop with 2 moderate impedance nodes; stability might be a major issue for high frequency and high-gain applications. Therefore, its F_{GBW} is relatively low for this application. Table 2 shows that the proposed VGA presents very good performances for both bandwidth and linearity over most of the previously reported solutions. Power dissipation is relatively high in this work since all the subsections can handle large signal.

Conclusions

A low distortion high bandwidth VGA architecture has been proposed. Its variable gain range is 0–42 and –3 dB bandwidth is around 270 MHz. Additional fre-

quency compensation circuits improve its bandwidth by more than 60%. The VGA can handle signals up to 1 V_{pk-pk} with HD3 below than –55 dB. A single power supply voltage of 2.7 V is employed; maximum power consumption is 54 mW.

The proposed architecture is suitable for high-frequency low-distortion and low-voltage applications. Another important feature is that the VGA can be fabricated in pure digital CMOS technologies.

Acknowledgments

This work was partially supported by National Instruments.

References

1. J.J.F. Rijns, “CMOS low-distortion high-frequency variable-gain amplifier.” *IEEE J. Solid-State Circuits*, vol. 31, pp. 1029–1034, 1996.
2. V. Gopinathan, M. Tarsia, and D. Choi, “Design considerations and implementation of a programmable high-frequency continuous-time filter and variable-gain amplifier in submicrometer CMOS.” *IEEE J. Solid-State Circuits*, vol. 34, pp. 1698–1707, 1999.

3. A. Motamed, C. Hwang, and M. Ismail, "A low-voltage low-power wide-range CMOS variable gain amplifier." *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 7, pp. 800–811, 1998.
4. F. Piazza, P. Orsatti, Q. Huang, and H. Miyakawa, "A 2 mA/3 V 71 MHz IF amplifier in 0.4 μm CMOS programmable over 80 dB range." *IEEE ISSCC 1997*, pp. 78–79, 434, 1997.
5. P.-C. Huang, L.-Y. Chiou, and C.-K. Wang, "A 3.3-V CMOS wideband exponential control variable-gain-amplifier." *IEEE IS-CAS 1998*, vol. 1, pp. 285–288, 1998.
6. W.C. Song, C.J. Oh, G.H. Cho, and H.B. Jung, "A 200 MHz/90 dB gain range CMOS VGA," in *Proc. 2nd IEEE Asia Pacific Conf. ASICs (AP-ASIC)*, 2000, pp. 1–4.
7. T. Yamaji, N. Kanou, and T. Itakura, "A temperature stable CMOS variable-gain amplifier with 80-dB linearly controlled gain range." *IEEE J. Solid-State Circuits*, vol. 37, pp. 553–558, 2002.
8. G. Han and E. Sanchez-Sinencio, "CMOS transconductance multipliers: A tutorial." *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 12, pp. 1550–1563, 1998.
9. R.A. Balmford and W. Redman-White, "New high-compliance CMOS current mirror with low harmonic distortion for high frequency circuits." *IEE Electronics Letters*, vol. 29, pp. 1738–1739, 1993.
10. K. Philips and E.C. Dijkmans, "A variable gain IF amplifier with -67 dBc IM/sub 3/-distortion at 1.4 V/sub pp/ output in 0.25/ μm CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2001, pp. 81–82.



Siang Tong Tan received the B.S. degree from National Taiwan University, Taiwan, R.O.C., in 1998 and the M.S. degree from Texas A&M University, College Station, TX, in 2001, both in electrical engineering. He then joined the Storage Products Group of Texas Instruments, Dallas, TX, to work on preamplifier design for hard-disk-drive. His research interests include wide-band, high-speed CMOS and BiCMOS analog building blocks.



José Silva-Martínez was born in Tecamachalco, Puebla, México. He received the M.Sc. degree from the Instituto Nacional de Astrofísica Óptica y Electrónica (INAOE), Puebla, México, in 1981, and the Ph.D. degree from the Katholieke Univesiteit Leuven, Belgium in 1992.

From 1981 to 1983, he was with the Electrical Engineering Department, INAOE, where he was involved with switched-capacitor circuit design. In 1983, he joined the Department of Electrical Engineering, Universidad Autónoma de Puebla, where he remained until 1993; He was a co-founder of the graduate program on Opto-Electronics in 1992. From 1985 to 1986, he was a Visiting Scholar in the Electrical Engineering Department, Texas A&M University. In 1993, he re-joined the Electronics Department, INAOE, and from May 1995 to December 1998, was the Head of the Electronics Department; He was a co-founder of the Ph.D. program on Electronics in 1993. He is currently with the Department of Electrical Engineering (Analog and Mixed Signal Center) Texas A&M University, at College Station, where He holds the position of Associate Professor.

Dr. Silva-Martínez has served as IEEE CASS Vice President Region-9 (1997–1998), and as Associate Editor for IEEE Transactions on Circuits and Systems part-II from 1997–1998 and May 2002 till present. He was the main organizer of the 1998 and 1999 International IEEE-CAS Tour in region 9, and Chairman of the International Workshop on Mixed-Mode IC Design and Applications (1997–1999). His current field of research is in the design and fabrication of integrated circuits for communication and biomedical applications. He is the inaugural holder of the TI Professorship-I in Analog Engineering, Texas A&M University. He was a co-recipient of the 1990 European Solid-State Circuits Conference Best Paper Award.