

# Calibration of Phase and Gain Mismatches in Weaver Image-Reject Receiver

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**Abstract**—A modified image-reject Weaver architecture is presented. The design automatically calibrates for phase and gain mismatches that limit the performance of image-reject receivers. On-line or off-line calibrations are possible without using any calibrating tone. An experimental CMOS prototype RF front-end operating at 1.8 GHz achieves an image rejection ratio of 59 dB using on-line calibration. The design was fabricated in a 0.35- $\mu\text{m}$  CMOS process and dissipates 160 mW from a 3-V supply during on-line calibration, and 95 mW during normal receiving. The die area is 4 mm<sup>2</sup>.

**Index Terms**—CMOS RF circuits, gain mismatch, image-reject receiver, phase mismatch, receiver calibration, Weaver architecture.

## I. INTRODUCTION

THE image-reject receiver is an architecture that passes the signal of interest and rejects the image signal, therefore, it is a good choice for receiver integration as there is no need ideally for an image-reject filter. Moreover, power consumption can be greatly reduced because there is no need to drive a low input impedance off-chip passive filter. Another advantage is that the choice of the IF frequency can be very low because the performance of image rejection does not depend on IF as in heterodyne receivers. Therefore, selectivity is sufficient with integrated filters with a quality factor  $Q$  in the range of 10–20.

Typical image-reject receivers are Weaver and Hartley architectures. Due to mismatches between the two signal paths in these architectures, the image reject ratio (IRR) is limited to around 30–40 dB for 1–5° phase mismatch or 0.2–0.6 dB gain mismatch [1]. For example, the conventional  $RC$ - $CR$  network used in Hartley architecture is based on achieving 90° phase difference between a pole and a zero with the same cutoff frequency. Due to its asymmetric structure, the phase accuracy of the  $RC$ - $CR$  quadrature generator network is small. Only with tuning and trimming can its phase error be made lower than 1°. Also, equal gain is achieved only at  $\omega = (1/(RC))$ , and therefore, gain error occurs at frequencies relatively far from this frequency. Therefore, the IRR is limited, and the amplitude and phase errors are highly sensitive to absolute variation of the  $R$  and  $C$  values. This will put a restriction on the system specifications by attenuating the image signal using an off-chip image-reject filter preceding the mixer stage. Other image-reject techniques include single and double quadrature downcon-

version, which depend on using polyphase filters to reject the image signal [2]–[5]. For low-IF receivers, the required  $R$  and  $C$  values are large and require a large die area.

To achieve complete receiver integration on-chip, especially for the RF part, improved and innovative architectures are needed. Special dedicated tone (at image frequency) can be used in calibrating the receiver for these mismatches. Periodic calibration with the external image tone is needed [6]. This property restricts its applications on systems like time-division multiple-access (TDMA). Digitally storing the calibration coefficients solves the problem of periodic calibration, however, an external image tone is still needed in the calibration [7].

In this modified Weaver receiver, phase and gain mismatches are independently calibrated without the use of any external calibrating tones. Calibration can be done continuously on-line with some restrictions, or only one time to generate the correction signals and storing them digitally. In Section II, the receiver architecture and the calibration system are analyzed. Section III explains the circuit design in CMOS technology of each building block. Some nonideal issues that affect the calibration accuracy are discussed in Section IV. Experimental measurements results are reported in Section V.

## II. RECEIVER ARCHITECTURE

### A. Modeling of Phase and Gain Mismatches

Fig. 1 shows the Weaver image-reject receiver together with extra multiplication blocks required to generate phase and gain error signals. In order to calibrate for the mismatches in the architecture, phase and gain mismatches are distributed in a symmetric way to simplify the analysis [8]. The phase mismatches of the architecture are distributed as  $\theta_1$  and  $\theta_2$  for the first and second local oscillator (LO), respectively. Similarly, the gain mismatches are distributed as  $\Delta A_1$  and  $\Delta A_2$  for each LO. The output of this architecture for an image tone  $\cos(\omega_{\text{IM}}t)$  can be calculated by tracking the signals at the outputs of the filters and IF mixers as shown in Equations (1–2), where  $\omega_{\text{IM}} = \omega_1 - \omega_2 \pm \omega_{\text{IF}}$ ,  $A = A_1 A_2$ ,  $\theta = \theta_1 + \theta_2$ , and  $\Delta A = \Delta A_1 A_2 + \Delta A_2 A_1$ . On the other hand, the output of the architecture to RF tones,  $\omega_{\text{RF}} = \omega_1 + \omega_2 \pm \omega_{\text{IF}}$ , is given by Equation (3). A simple  $LC$  notch filter can remove one of the RF tones before being introduced at the input of the architecture, thus a single desired RF channel passes through the architecture.

### B. Calibrating System

The IRR is a function of the phase mismatch  $\theta$  and the gain mismatch  $\Delta A$ . The values of mismatches need to be very small to achieve an acceptable IRR without the necessity of using

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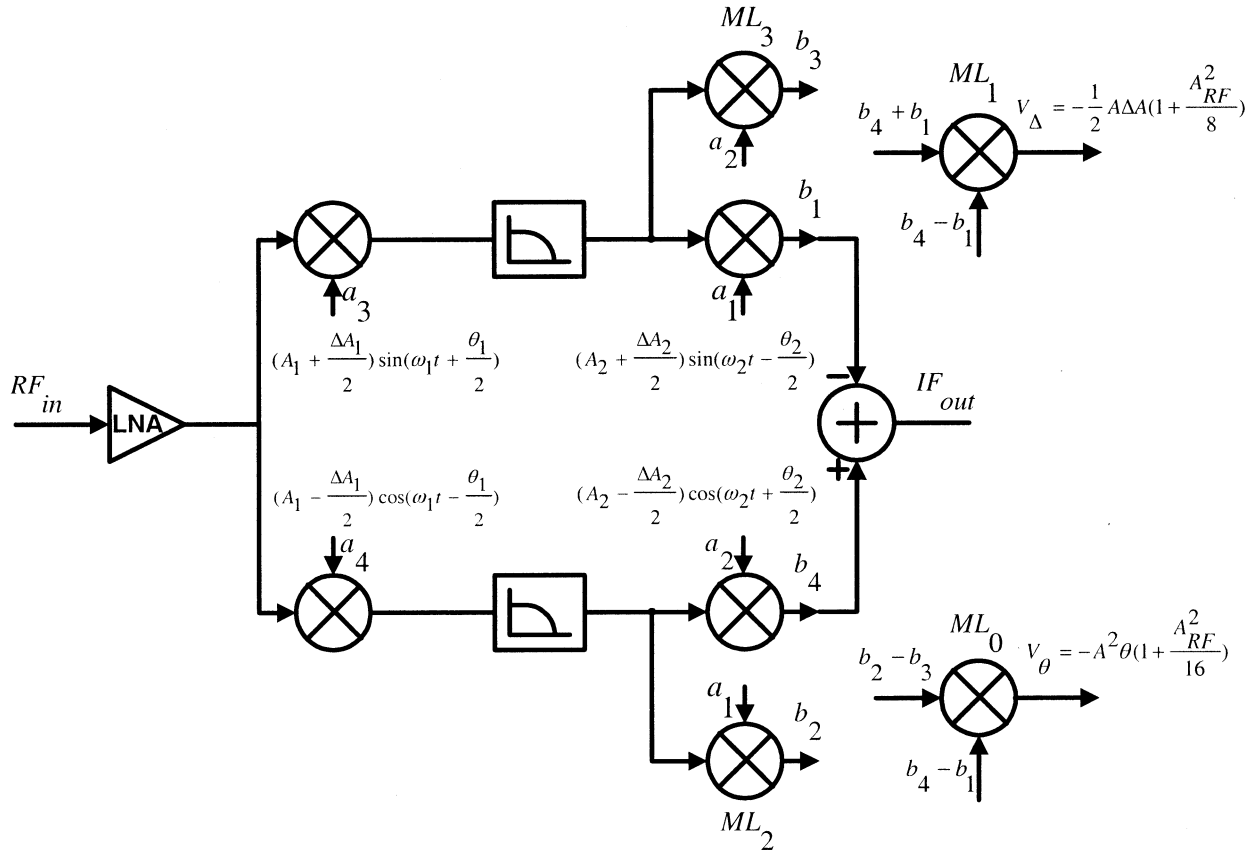


Fig. 1. Modeling and generating error signals in Weaver architecture.

an off-chip image-reject filter. A calibrating system is required to calibrate for these mismatches. This system generates two control signals to correct for both phase and gain mismatches using a variable delay-gain circuit in two independent calibration loops. The loops adjust  $\theta_2$  and  $\Delta A_2$  until both  $\theta$  and  $\Delta A$  settle to zero. In this case, the output signal in (2) due to the image signal will be zero.

The calibrating system is shown in Fig. 2, where the LO signals  $a_1 \dots a_4$  are processed to obtain two error signals related to the phase and gain mismatches. Two amplifiers with a high gain  $G$  amplify the error signals, represented as  $V_\theta$  and  $V_\Delta$ , in a closed-loop system to obtain two correction signals, represented as  $V_{c\theta}$  and  $V_{c\Delta}$ . The high output impedance of the amplifier circuit with a load capacitance at the output creates a dominant pole and acts as a low-pass filter (LPF) for the error signals. The correction signals are fed back to a variable delay-gain circuit

to adjust the phase and gain mismatches of the second LO quadrature outputs, thus, completing the closed loops. The two high-gain amplifiers in this system force the final values of the error signals inside the loop to be zero, which guarantees almost ideal image rejection performance.

The phase and gain error signals are extracted from the receiver as shown in Fig. 1. Two extra multipliers are used in generating the signals  $b_1 \dots b_4$ , which contains information about the phase and gain mismatches in the receiver. Another two extra multipliers are used in processing the signals  $b_1 \dots b_4$  to obtain the phase and gain error signals  $V_\theta$  and  $V_\Delta$ . The calibrating system and the error signals generation system depend on multiplying the first and second LO signals to obtain the signals  $b_1 \dots b_4$ . Therefore, the RF mixers outputs must contain a component for the first LO quadrature signals. This can be achieved by using single-balanced design for the RF mixers.

$$\left. \begin{aligned} X_A(t) &= \frac{1}{2} \left( A_1 + \frac{\Delta A_1}{2} \right) \sin \left( (\omega_1 - \omega_{IM})t + \frac{\theta_1}{2} \right) \\ X_B(t) &= \frac{1}{2} \left( A_1 - \frac{\Delta A_1}{2} \right) \cos \left( (\omega_1 - \omega_{IM})t - \frac{\theta_1}{2} \right) \\ X_C(t) &= \frac{1}{4} \left( A_1 + \frac{\Delta A_1}{2} \right) \left( A_2 + \frac{\Delta A_2}{2} \right) \cos \left( \omega_{IF}t - \frac{\theta}{2} \right) \approx \frac{1}{4} \left( A + \frac{\Delta A}{2} \right) \cos \left( \omega_{IF}t - \frac{\theta}{2} \right) \\ X_D(t) &= \frac{1}{4} \left( A_1 - \frac{\Delta A_1}{2} \right) \left( A_2 - \frac{\Delta A_2}{2} \right) \cos \left( \omega_{IF}t + \frac{\theta}{2} \right) \approx \frac{1}{4} \left( A - \frac{\Delta A}{2} \right) \cos \left( \omega_{IF}t + \frac{\theta}{2} \right) \end{aligned} \right\} \quad (1)$$

$$X_{out}(t) = \frac{1}{4} \left( \left( A - \frac{\Delta A}{2} \right) \cos \left( \omega_{IF}t + \frac{\theta}{2} \right) - \left( A + \frac{\Delta A}{2} \right) \cos \left( \omega_{IF}t - \frac{\theta}{2} \right) \right) \quad (2)$$

$$X_{out}(t) = \frac{1}{4} \left( \left( A - \frac{\Delta A}{2} \right) \cos \left( \omega_{IF}t + \frac{\theta}{2} \right) + \left( A + \frac{\Delta A}{2} \right) \cos \left( \omega_{IF}t - \frac{\theta}{2} \right) \right). \quad (3)$$

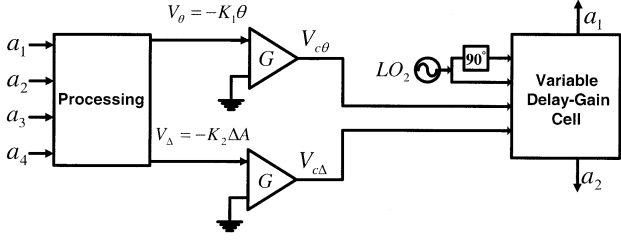


Fig. 2. Phase and gain calibrating system.

Neglecting the effect of the low-pass filters and assuming a zero input to the system for simplicity in the analysis (by disconnecting the low-noise amplifier (LNA) output from the RF mixers inputs), these signals can be written as shown in Equation (4). An error signal proportional to the phase mismatch  $\theta$  is obtained by multiplying  $(b_4 - b_1)$  by  $(b_2 - b_3)$  and low-pass filtering the output. This can be written as

$$\begin{aligned} V_\theta &= \text{LPF}((b_4 - b_1)(b_2 - b_3)) \\ &= \text{LPF}(b_1b_3 - b_1b_2 + b_4b_2 - b_4b_3) = -\frac{1}{2}A^2\theta. \end{aligned} \quad (5)$$

Similarly, an error signal proportional to the gain mismatch  $\Delta A$  is obtained by multiplying  $(b_4 - b_1)$  by  $(b_4 + b_1)$  and low-pass filtering the output. The corresponding equation is

$$\begin{aligned} V_\Delta &= \text{LPF}((b_4 - b_1)(b_4 + b_1)) \\ &= \text{LPF}(b_4^2 - b_1^2) = -\frac{1}{2}A\Delta A. \end{aligned} \quad (6)$$

These expressions are assumed for the off-line calibration case ( $A_{\text{RF}} = 0$ ). In this case, a switch disconnects the LNA from the mixer input and calibration is to be done independent of the input signal.

Another calibration mode is to calibrate on-line. Assuming an RF signal  $A_{\text{RF}} \cos(\omega_{\text{RF}}t)$ , it can be shown that the corresponding error signals can be written as

$$V_\theta = -\frac{1}{2}A^2\theta \left(1 + \frac{A_{\text{RF}}^2}{16}\right) \quad (7)$$

$$V_\Delta = -\frac{1}{2}A\Delta A \left(1 + \frac{A_{\text{RF}}^2}{8}\right). \quad (8)$$

Thus, for small input signals (e.g., less than  $-25$  dBm), the error signals can be approximated to the off-line case.

### C. Self-Calibrated Architecture

According to the above analysis, the signal  $V_{c\theta}$  can be used in a closed calibration loop to adjust the phase mismatch of the quadrature outputs from  $\text{LO}_2$  using a variable delay circuit until  $\theta$  approaches zero. Similarly, the signal  $V_{c\Delta}$  can be used in adjusting the gain of the quadrature outputs from  $\text{LO}_2$  until  $\Delta A$

approaches zero. The actual implementation of the image-reject architecture with compensation signals generation is shown in Fig. 3. In this implementation, we used four extra multipliers ( $\text{ML}_0$  to  $\text{ML}_3$ ) and two amplifiers to correct for mismatches. The two high gain amplifiers force  $\theta$  and  $\Delta A$  to settle down to a zero reference value. Phase and gain compensation can be done in two different ways:

- 1) In the slots of time where the mixer is not in receiving mode (off-line), as in TDMA systems, a dc input (normal bias) is applied to the mixer input using a switch to disconnect the RF input. This will generate all the required control signals using (5) and (6). The compensation signals are stored on capacitors to compensate for the mismatches when the mixer is in receiving mode. This means that no power consumption or noise addition will be added in receiving mode (except of those of the variable delay and gain circuits). Also, calibration can be done one-time and the correction signals are stored digitally. In both cases, the calibration loops are independent of the input RF signal.
- 2) Calibration is done all the time (on-line) by closing the switches in Fig. 3. In this case, the control signals are generated according to (7) and (8). For small input RF power, these equations can be approximated to (5) and (6).

## III. CIRCUIT IMPLEMENTATION

The design is differential, including mixers, LPFs, a variable delay-gain circuit, and amplifiers. Addition and subtraction are implemented by adding or subtracting currents, which can be done in the multipliers implicitly by cross-coupling differential output branches. In the following, a description of each building circuit is presented.

### A. Variable Delay-Gain Circuit

The phase and gain correction signals are applied to the variable delay-gain circuit shown in Fig. 4. The output of the circuit is a combination of two paths from the input with different delays. The transfer function of this circuit can be calculated using superposition to be

$$\frac{V_o(s)}{V_{\text{in}}(s)} = g_{m3}R_L \frac{s - \frac{1}{C_0} \left( \frac{g_{m1}g_{m2}}{g_{m3}} - g_{m0} \right)}{s + \frac{g_{m0}}{C_0}} \quad (9)$$

where  $g_{m_i}$  is the transconductance of transistor pair  $M_i$ . At the special case of  $g_m = g_{m3} = g_{m2}$  and  $g_{m1} = 2g_{m0}$ , (9) becomes an all-pass filter transfer function in the following form:

$$\frac{V_o(s)}{V_{\text{in}}(s)} = g_m R_L \frac{s - \frac{g_{m0}}{C_0}}{s + \frac{g_{m0}}{C_0}}. \quad (10)$$

$$\left. \begin{aligned} b_1 &\approx \frac{1}{2} \left( A + \frac{\Delta A_1 A_2 + \Delta A_2 A_1}{2} \right) \left( \cos((\omega_1 - \omega_2)t + \frac{\theta_1 + \theta_2}{2}) - \cos((\omega_1 + \omega_2)t + \frac{\theta_1 - \theta_2}{2}) \right) \\ b_2 &\approx -\frac{1}{2} \left( A - \frac{\Delta A_1 A_2 - \Delta A_2 A_1}{2} \right) \left( \sin((\omega_1 - \omega_2)t - \frac{\theta_1 - \theta_2}{2}) - \sin((\omega_1 + \omega_2)t - \frac{\theta_1 + \theta_2}{2}) \right) \\ b_3 &\approx \frac{1}{2} \left( A + \frac{\Delta A_1 A_2 - \Delta A_2 A_1}{2} \right) \left( \sin((\omega_1 - \omega_2)t + \frac{\theta_1 - \theta_2}{2}) + \sin((\omega_1 + \omega_2)t + \frac{\theta_1 + \theta_2}{2}) \right) \\ b_4 &\approx \frac{1}{2} \left( A - \frac{\Delta A_1 A_2 + \Delta A_2 A_1}{2} \right) \left( \cos((\omega_1 - \omega_2)t - \frac{\theta_1 + \theta_2}{2}) + \cos((\omega_1 + \omega_2)t - \frac{\theta_1 - \theta_2}{2}) \right) \end{aligned} \right\} \quad (4)$$

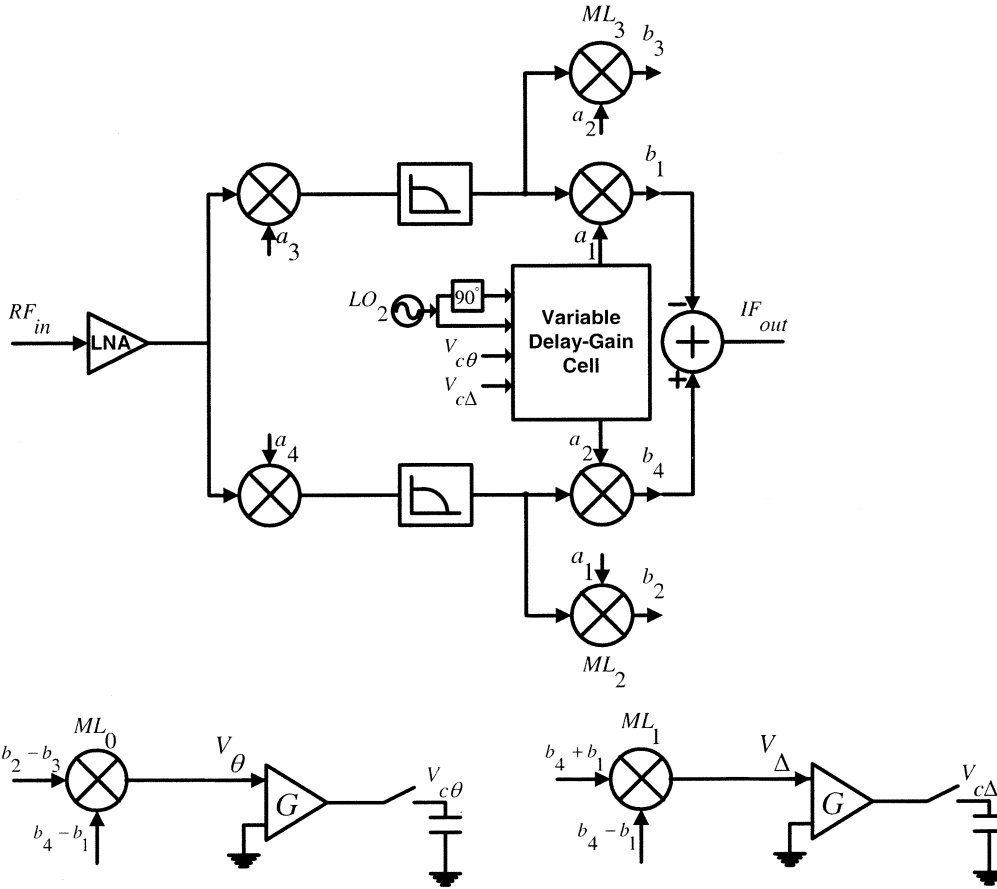


Fig. 3. Self-calibrated Weaver image-reject architecture.

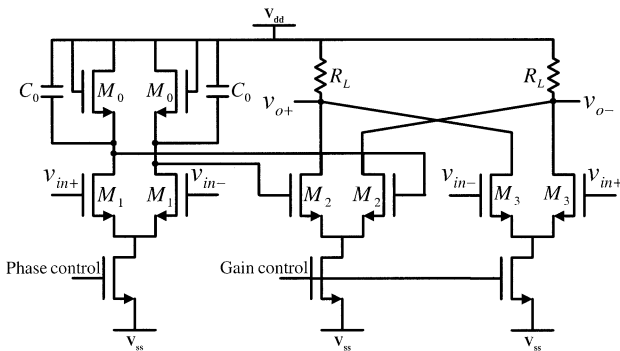


Fig. 4. Variable delay-gain circuit.

The phase correction signal adjusts the pole and zero locations by changing the value of  $g_{m0}$ , while the gain control signal adjusts the dc gain of the filter by changing the value of  $g_m$ , without interfering with each other. This feature makes it possible for simultaneous phase and gain calibration.

### B. LNA and RF Mixer Circuits

To have a complete RF front-end and get a better understanding about how much the architecture can correct the IRR in a receiver front-end, we used the cascode LNA and RF mixer circuits shown in Fig. 5. The LNA has a good isolation between the input and output ports, and can achieve a high gain. The LNA

load resonates at the desired frequency range and attenuates the image frequency by few decibels.

The RF mixer is a single-balanced circuit. The  $LO_1$  input signal to the mixer is a large amplitude sinusoid. The RF signal is coupled to the gates of the transconductance transistors through a coupling capacitor. Using large-amplitude LO signals help reduce the noise contribution of the switching transistors.

The input transconductance transistor converts the input RF voltage signal into a current which is switched differentially by the LO signals. The IF current is converted back into a voltage signal through the load resistors  $R_L$ . The switching operation is equivalent to multiplying the RF current by a square-wave signal  $S(t)$  toggling between  $-1$  and  $1$ . The signal  $S(t)$  can be written as a summation of its harmonics as

$$S(t) = \frac{4}{\pi} \cos(\omega_{LO}t) + \frac{4}{3\pi} \cos(3\omega_{LO}t) + \frac{4}{5\pi} \cos(5\omega_{LO}t) + \dots \quad (11)$$

For single-balanced topology, the output IF current can be written as

$$I_{IF} = (I_{Bias} + g_m v_{RF}) S(t). \quad (12)$$

Due to  $I_{Bias}$  term, the output of a single-balanced mixer has a component for the LO signal, which is used in the calibration loops.

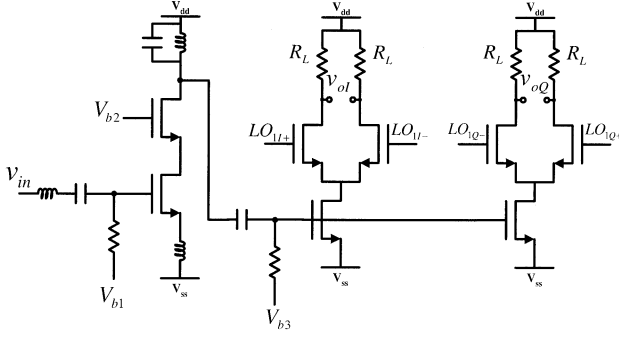


Fig. 5. LNA and RF mixer circuits.

### C. IF Multiplier Circuit

Transconductance multipliers can be implemented in different ways [9]. The IF multipliers and all other multipliers used in the calibration loops are implemented using the circuit shown in Fig. 6. This circuit was reported in [10] as an implementation for an RF multiplier circuit, and therefore it is a suitable implementation for the IF multipliers. The idea is to use six combiner circuits to implement a multiplier function. Each combiner circuit composes of two transistors connected together at their drains and loaded with a resistor. The output voltage of the multiplier circuit can be expressed as

$$v_o = -32R_cR_d^2K_cK_d^2(X - V_T)(Y - V_T)xy \quad (13)$$

where  $K$  is the transconductance parameter,  $x$  and  $y$  are the input signals to the multiplier, and  $X$  and  $Y$  are their dc voltage levels. The derivation of (13) is based on the assumption of perfect square-law MOSFET characteristics and completely matched devices. However, nonideal effects such as mobility degradation and channel length modulation effects and device mismatches due to process variations introduce extra higher order terms in the multiplication function and are analyzed in [10].

### D. Amplifier Circuit

The amplifiers used in the calibration loops are implemented as folded cascode circuit, which is characterized by its high gain and large output impedance. A load capacitance of 15 pF is added at each output node. The derivation of the phase and gain error signals in (7) and (8) is based on the assumption of low-pass filtering the corresponding multiplication terms. The folded cascode circuit with its high output impedance acts as an LPF and stabilizes the two closed loops.

## IV. NONIDEAL EFFECTS

Some nonideal effects need to be considered in order to achieve good image rejection performance. One factor that determines the accuracy of calibration is the offset of the amplifier circuit in each calibration loop. In this case, a design with offset cancellation technique is preferred. As an example, for an offset of 5 mV, closed-loop gain of 10, and assuming that the variable delay-gain circuit corrects for  $1^\circ/0.1$  V of phase calibration, then a phase error of  $0.5^\circ$  is caused by the

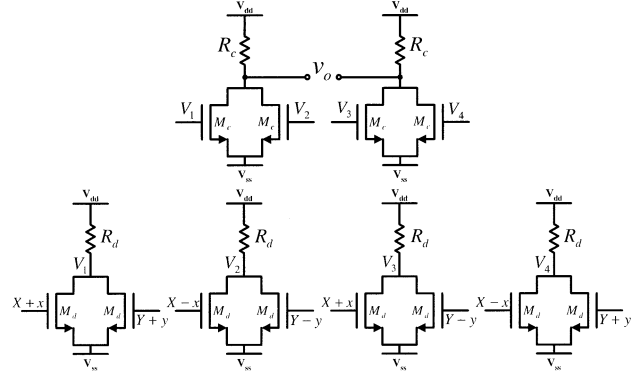


Fig. 6. IF multiplier circuit.

amplifier offset. Similar calculations can be done for the effect on gain calibration.

The mismatches are dependent on the following factors:

- 1) Actual  $RC$  process variations of the  $90^\circ$  phase-shift passive network used in generating quadrature local oscillators.
- 2) RF mixer mismatches.
- 3) LPF mismatches.
- 4) IF multiplier mismatches.

In the architecture of Fig. 3, we neglect the effect of the last factor. This is justified by noting that the IF multipliers are operating at much lower frequency than the RF mixer. However, this effect can be minimized by proper layout techniques if the layout, of the two multipliers of the main receiver path, is repeated as one block for multipliers  $ML_2$  and  $ML_3$  of the calibration loops. In this case, the relative mismatches for each pair of IF multipliers are approximately the same. This means that the mismatch of these two extra multipliers is correlated with the mismatch of the multipliers in the main receiver path. To mathematically model this correlation, let us assume that the phase mismatch of the multipliers  $ML_2$  and  $ML_3$  equals to

$$\bar{\theta}_2 = \alpha_c \theta_2 + (1 - \alpha_c) \theta_{2uc} \quad (14)$$

where  $\alpha_c$  is the correlation factor between  $\bar{\theta}_2$  and  $\theta_2$ , and  $\theta_{2uc}$  is the uncorrelated part of  $\bar{\theta}_2$  with  $\theta_2$ . By performing the same analysis procedure, we can derive the following phase error signal:

$$V_\theta = \frac{1}{2} A^2 \left( \theta_1 + \frac{1 + \alpha_c}{2} \theta_2 + \frac{1 - \alpha_c}{2} \theta_{2uc} \right). \quad (15)$$

Thus, the closed loop will adjust  $V_\theta$  to approach zero when

$$\theta_2 = -\frac{2}{1 + \alpha_c} \theta_1 - \frac{1 - \alpha_c}{1 + \alpha_c} \theta_{2uc} \quad (16)$$

and the compensation will correct  $\theta_2$  according to (16). If  $\alpha_c = 1$ , then there is a complete correlation between the phase mismatches of the multipliers and the compensation will be completely correct. A similar analysis can be done for the gain mismatch.

To minimize the sensitivity of the calibration loops and maintain a constant large image rejection performance (especially for

on-line calibration), the variable delay-gain circuit should be designed to correct small phase and gain mismatches by relatively large correction signals. Also, the interaction between the phase and gain correction loops should be minimized to reduce the sensitivity of the circuit. Possible solutions are to correct for part of the gain of the  $LO_2$  signals or correct the gain in the main receiver path and correct only the phase of the  $LO_2$  signals.

## V. MEASUREMENT RESULTS

To prove the analysis and the calibration idea of the phase and gain mismatches, the self-calibrated Weaver receiver was implemented in a  $0.35\text{-}\mu\text{m}$  CMOS technology. The circuit was tested with a 3-V supply. The first and second LO frequencies were 1.6 GHz and 200 MHz, respectively. The choice of the IF frequency is optional, as the output is not sensitive to it. The desired RF signal was around 1.8 GHz, while its image signal was around 1.4 GHz. IRR performance was measured by applying a desired tone and an image tone of equal power and measuring the difference between their powers at the output.

Typical phase and gain mismatches limit the achievable IRR to 26 dB without calibration, as shown in Fig. 7. In this measurement, the two signals are slightly shifted for measurement purpose. After enabling on-line calibration, the same test was repeated as shown in Fig. 8, where the IRR improved to 59 dB. Fig. 9 shows the IRR performance as a function of  $LO_1$  frequency, for a fixed IF output frequency. The decrease in IRR for frequencies away from the calibration point ( $LO_1 = 1.6$  GHz) is due to the nonideal effects discussed in Section IV.

The dynamic range of the input RF signal can vary widely. On-line calibration is valid for RF input power below  $-25$  dBm at the LNA input. Above this value, the IRR decreases rapidly. If the calibration is to be done only one time and the correction signals are to be stored digitally, then the IRR will not depend on the input power level. The measured input 1-dB compression point is  $-15$  dBm. The receiver consumes 160 mW during on-line calibration and 95 mW during normal receiving.

A comparison between this technique and two calibration loops based techniques is shown in Table I. Unlike the other techniques, this design does not need a calibrating tone, and it can calibrate both on-line and off-line. The power consumption of this design is between those reported in [6] and [7]. The IF multipliers consume a large section of the total power. A summary of the measurements of the fabricated image-reject receiver is shown in Table II. The  $2 \times 2$  mm<sup>2</sup> chip die micrograph is shown in Fig. 10.

## VI. CONCLUSION

A self-calibrated image-reject receiver has been introduced. More integration on-chip can be achieved as the architecture is designed to be insensitive to mismatches, and the off-chip image-reject filter can be removed. Independent phase and gain calibrations for Weaver image-reject receiver were presented. The main advantage of this design over other reported techniques is the possibility of calibrating the receiver on-line and without using an image tone for calibration. An experimental prototype in a  $0.35\text{-}\mu\text{m}$  CMOS process indicates an improvement in the measured IRR from 26 to 59 dB before and after cal-

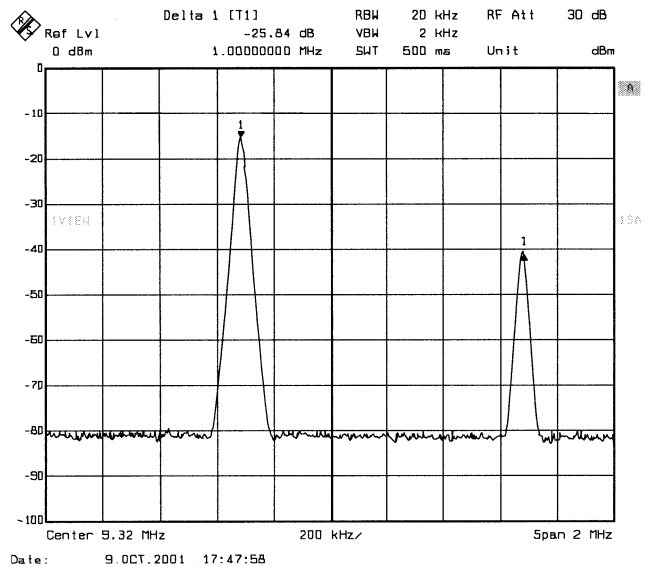


Fig. 7. Output spectrum (signal and image tones) without calibration.

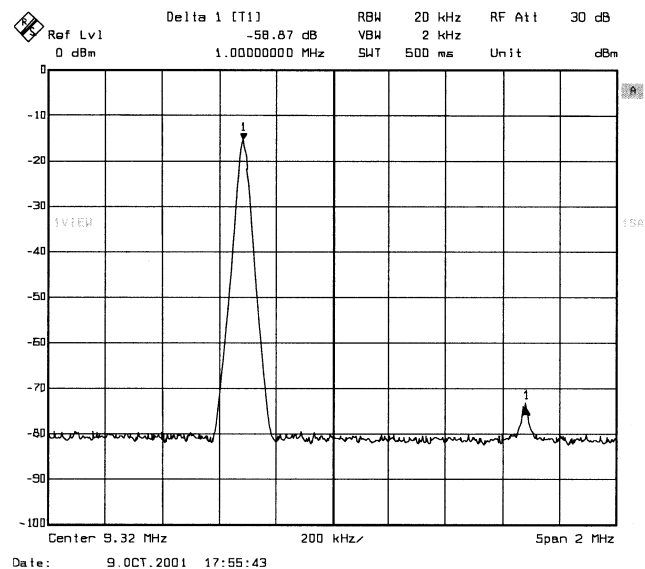


Fig. 8. Output spectrum with on-line calibration.

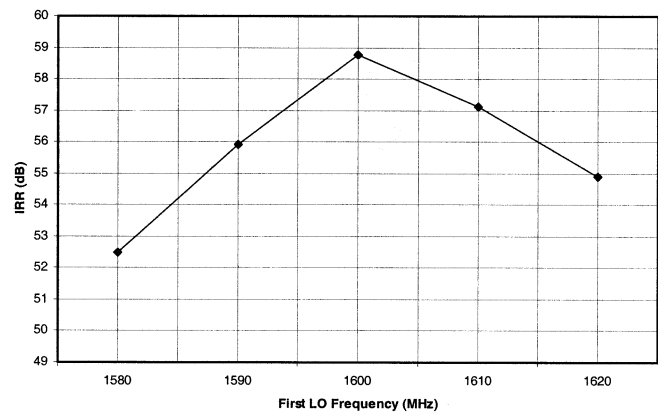


Fig. 9. Measured IRR as a function of  $LO_1$  frequency.

TABLE I  
A COMPARISON BETWEEN CLOSED-LOOP CALIBRATION TECHNIQUES FOR MISMATCHES

Parameter	Ref. [6]	Ref. [7]	This work
Technology	0.35 $\mu$ m CMOS	0.25 $\mu$ m CMOS	0.35 $\mu$ m CMOS
Supply voltage	3V	2.5V	3V
Power consumption (normal reception)	105mW	50mW	95mW
Power consumption (calibration)	170mW	55mW	160mW
Phase calibration		√	√
Gain calibration	√	√	√
Calibrating tone	√	√	
Off-line calibration	√	√	√
On-line calibration			√

TABLE II  
SUMMARY OF THE RECEIVER MEASUREMENTS

Parameter	Measurement
LO <sub>1</sub> frequency	1.6GHz
LO <sub>2</sub> frequency	200MHz
RF frequency	Around 1.8GHz
Image frequency	Around 1.4GHz
IRR (before calibration)	26dB
IRR (after calibration)	59dB
Input 1dB compression point	-15dBm
Supply voltage	3V
Power consumption	95mW

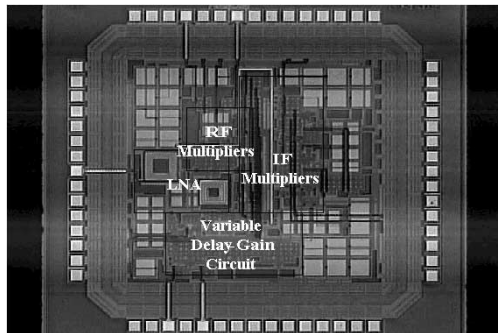


Fig. 10. Die photo of the self-calibrated Weaver receiver.

ibration. Thus, the main problem associated with the image-rejection receiver can be solved using this technique.

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