

# A $2\text{-}V_{pp}$ 80–200-MHz Fourth-Order Continuous-Time Linear Phase Filter With Automatic Frequency Tuning

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**Abstract**—A CMOS 80–200-MHz fourth-order continuous-time  $0.05^\circ$  equiripple linear phase filter with an automatic frequency tuning system is presented. An operational transconductance amplifier based on transistors operating in triode region is used and a circuit that combines common-mode feedback, common-mode feedforward, and adaptive bias is introduced. The chip was fabricated in a  $0.35\text{-}\mu\text{m}$  process; filter experimental results have shown a total harmonic distortion less than  $-44$  dB for a  $2\text{-}V_{pp}$  differential input with a single  $2.3\text{-V}$  power supply. The group delay ripple is less than 4% for frequencies up to  $1.5 f_c$ . The frequency tuning error is below 5%.

**Index Terms**—Adaptive bias, common-mode feedback (CMFB), common-mode feedforward (CMFF), low voltage, OTA-C filters, pseudodifferential amplifiers.

## I. INTRODUCTION

FOR APPLICATIONS of low power-supply voltages and large signal swings, pseudodifferential structures are attractive since they avoid the voltage drop across the tail current source, but inherently pseudodifferential structures have the same low-frequency transconductance for both differential and common-mode signals. Therefore, the use of pseudodifferential structures requires a careful and efficient control over the common-mode (CM) behavior of the circuits [1]–[5]. For tunable filters and other differential systems, an adaptive mechanism is also needed to control the CM behavior over the tuning range [5].

In this paper, the design of a pseudodifferential operational transconductance amplifier (OTA), optimized for linearity performance, is discussed. A CM control circuit which integrates common-mode feedforward (CMFF), common-mode feedback (CMFB), and adaptive bias into one circuit is proposed. A wide tunable range linear phase filter based on the OTA and the CM control circuit is designed. A simple but efficient automatic frequency tuning system is used to compensate filter deviations due to the process and temperature variations. The filter can be used in the 1000Base-T systems as the antialiasing filter.

## II. PSEUDODIFFERENTIAL TRANSCONDUCTOR

The pseudodifferential self-regulated OTA based on transistors operating in triode region is shown in Fig. 1 [6]. Transistors M1 operate in triode region. Transistor M2 and ampli-

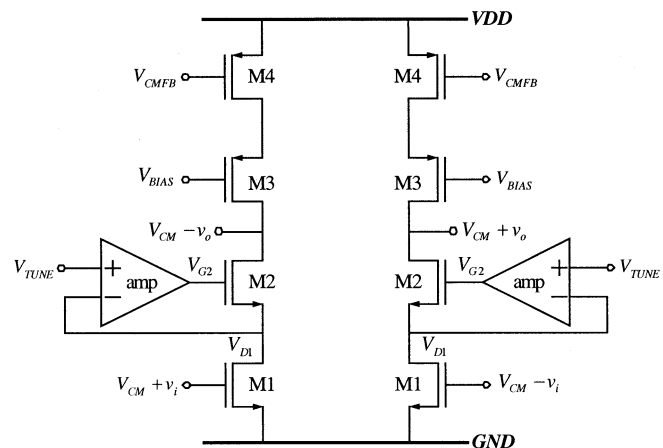


Fig. 1. Pseudodifferential OTA.

fier (amp) form a regulated gain-control (RGC) loop, and they are used to fix the drain voltage of M1. The tuning voltage  $V_{TUNE}$  is used to adjust the OTA's transconductance. Assuming an ideal amplifier, then we have both a constant drain–source voltage  $v_{DS1} = V_{TUNE}$  independent of the input voltage level, and a linear transconductance given by  $\beta_1 V_{TUNE}$ , where  $\beta_1 = \mu_n C_{ox}(W/L)_1$ .

Let us assume that  $V_{CM}$  is the CM reference voltage. Notice that M1 must operate in triode region and we need to support certain drain–source voltages  $V_{DSAT3}$  and  $V_{DSAT4}$  for M3 and M4, respectively. Hence, we can get the maximum signal swing and the required CM reference voltage if  $v_{i,max} = v_{o,max}$ , as

$$v_{i,max} = \frac{1}{2}(V_{DD} - V_{TN} - V_{TUNE} - V_{DSAT3} - V_{DSAT4}) \quad (1)$$

$$V_{CM} = V_{DD} - v_{i,max} - V_{DSAT3} - V_{DSAT4} \quad (2)$$

where  $V_{TUNE}$  is obtained from the required filter bandwidth and the transconductance of the OTA. The design of the RGC loop is critical for the OTA's linearity performance. One of the main sources of the OTA's nonlinearity is the low gain of the RGC loop at high frequencies. It can be shown that the third-order harmonic distortion (HD3) of the OTA output current (neglecting short-channel effects) can be expressed as

$$HD3 \cong \frac{V_i^2}{4} \cdot \frac{\beta_1^2}{[(A(s) + 1)g_{m2} + \beta_1(V_{CM} - V_{TN} - V_{D1})]^2} \quad (3)$$

where  $V_i$  is the magnitude of the input signal and  $A(s)$  is the gain of the RGC amplifier. Simulation results, in agreement with (3), show that the HD3 is dominated by  $(A(s)+1)g_{m2}$  if  $|A(s)| < 6$ . According to (3) and simulation results, to achieve total har-

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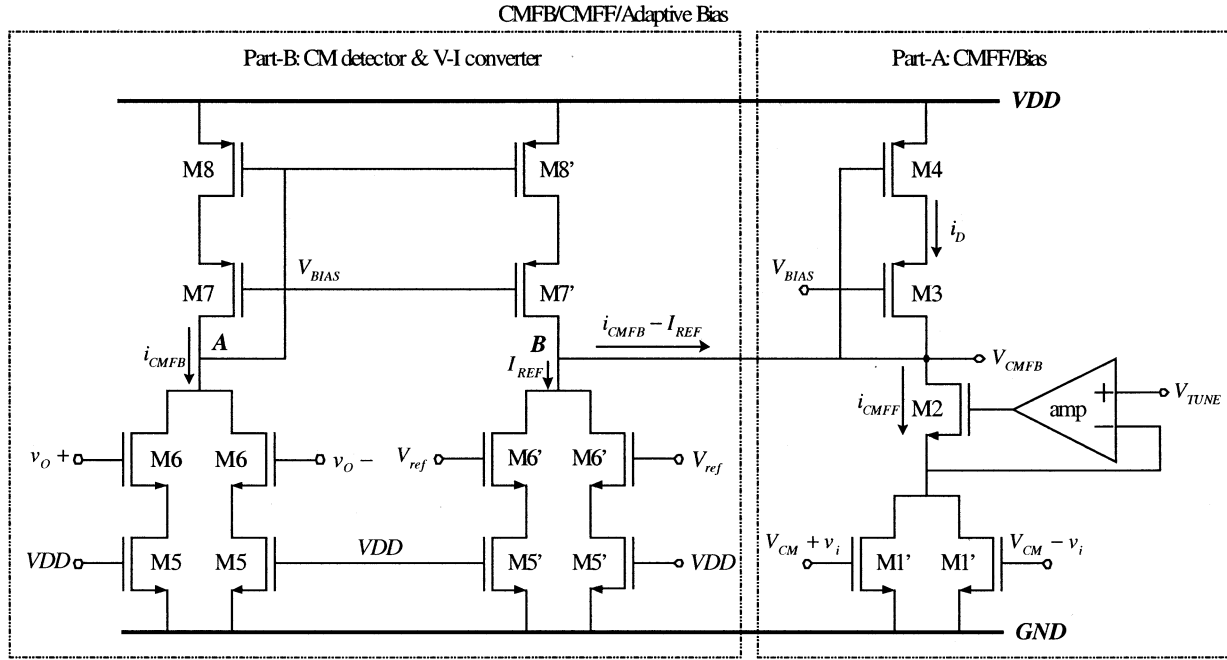


Fig. 2. Common-mode control circuit.

monic distortion (THD) figures of around  $-50$  dB, the RGC amplifier's gain should be greater than  $10$   $V/V$ . The implementation of the RGC amplifier is composed of a single-ended differential amplifier and a level shifter.

For short-channel devices, the effective carrier mobility  $\mu_{\text{eff}}$  is a function of both lateral and vertical electric fields [7]. While the lateral electric field effect is reduced by the RGC loop, which reduces the drain-source voltage variations, the vertical electric field effect is not. Higher level models show us that short-channel effects limit the OTA linearity; simulation results for different input transistor's length (with constant  $W/L$  ratio) give us an OTA's THD of less than  $-50$  dB for transistor lengths greater than  $0.6$   $\mu\text{m}$ .

### III. COMMON-MODE CONTROL

The OTA shown in Fig. 1 requires a proper CM control system. It should not only stabilize the OTA output CM voltage, but also reject the input CM signals and supply noise. So the combination of a CMFB and a CMFF for the CM control is essential for high-performance systems with pseudodifferential architectures.

The proposed CM control circuit senses the input CM information as well as the output CM information, then it combines both signals together to control the OTA's CM behavior. The implementation of the CM control is shown in Fig. 2. *Part A* is a CMFF and an adaptive bias circuit. The CMFF/Bias is a replica of a single branch of the OTA except that the dimensions of  $M1'$  are one half of the main OTA's input transistor ( $M1$  in Fig. 1). Transistor  $M1'$  are connected to the inputs of the OTA and driven by the tuning voltage; it is used to replicate the bias current and to cancel the CM input signals. The CMFF current is

$$i_{\text{CMFF}} = I_{\text{CMFF}} + 2g'_{m1}v_{\text{icm}} = I_{\text{CMFF}} + g_{m1}v_{\text{icm}} \quad (4)$$

where  $I_{\text{CMFF}}$  is the dc bias current with zero input CM signal and  $v_{\text{icm}}$  is the CM input signal. *Part B* of Fig. 2 is a CM detector and voltage-to-current converter. Transistors  $M6$  and  $M6'$  are driven by OTA outputs and the CM reference voltage, respectively. Transistors  $M5$  and  $M5'$  are working in deep triode region in order to improve the linearity of the CMFB. These circuits compare the output CM voltage with the reference CM voltage  $V_{\text{ref}}$  and convert the voltage difference into the CMFB correcting current:

$$i_{\text{cmfb}} \equiv i_{\text{CMFB}} - I_{\text{REF}} \cong \frac{2g_{m6}v_{\text{ocm}}}{1 + g_{m6}R_5} \quad (5)$$

where  $R_5$  is the effective drain-source resistance of  $M_5$ . Both the CMFB correcting current  $i_{\text{cmfb}}$  and CMFF current  $i_{\text{CMFF}}$  flow through transistors  $M3$  and  $M4$  and the overall current mirrored to the OTA output is

$$i_D = i_{\text{CMFF}} - i_{\text{cmfb}} = I_{\text{CMFF}} + g_{m1}v_{\text{icm}} - \frac{2g_{m6}v_{\text{ocm}}}{1 + g_{m6}R_5} \quad (6)$$

where  $I_{\text{CMFF}}$  provides the adaptive dc current,  $g_{m1}v_{\text{icm}}$  provides the CMFF correcting current, and  $2g_{m6}v_{\text{ocm}}/(1 + g_{m6}R_5)$  provides the current for the action of the CMFB.

A simplified open-loop equivalent circuit for the CMFB is shown in Fig. 3. There are three main poles at nodes  $A$ ,  $B$ , and  $C$ , and the CM loop gain  $A_{\text{CML}}(s)$  is approximated by

$$A_{\text{CML}}(s) = \frac{v'_{\text{ocm}}}{v_{\text{ocm}}} \cong \left( \frac{2g_{m6}}{(1 + g_{m6}R_5)g_{\text{oc}}} \right) \times \left[ \frac{1}{\left(1 + s\frac{C_A}{g_{m8}}\right) \left(1 + s\frac{C_B}{g_{m4}}\right) \left(1 + s\frac{C_C}{g_{\text{oc}}}\right)} \right] \quad (7)$$

where  $g_{\text{oc}} \cong 2(g_{\text{o3}}g_{\text{o4}}/g_{\text{m3}} + g_{\text{o1}}g_{\text{o2}}/(Ag_{\text{m2}}))$  is the output conductance at node  $C$ , and  $C_A$ ,  $C_B$ ,  $C_C$  are the total capac-

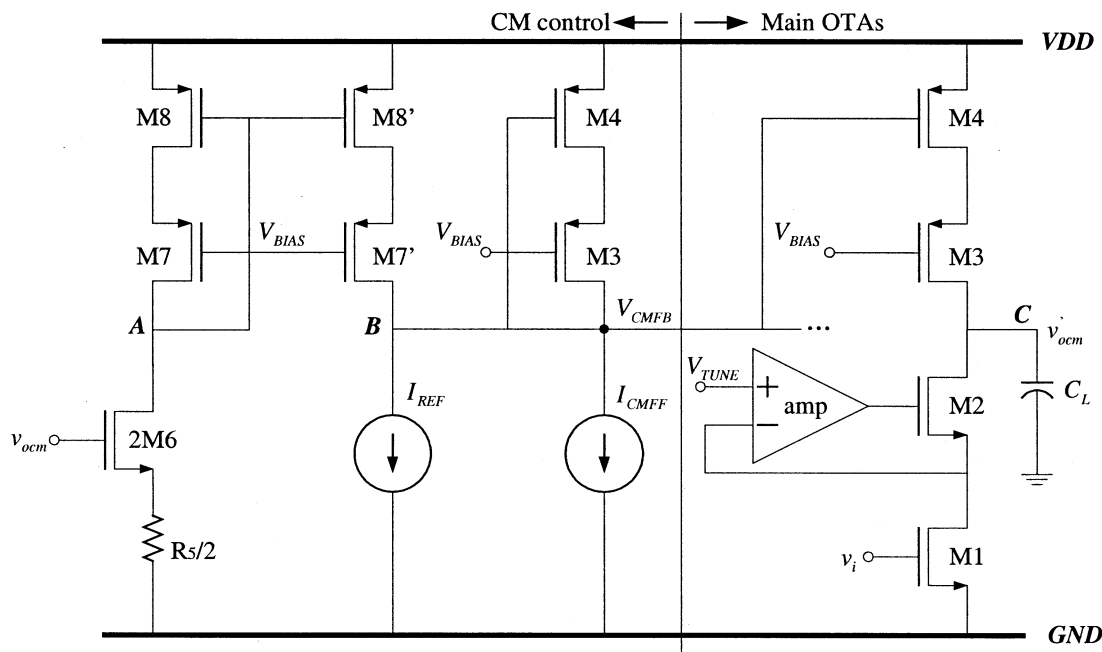


Fig. 3. Simplified CMFB open-loop equivalent circuit.

itances at the nodes *A*, *B*, and *C*, respectively. The factor 2 comes from the fact that the OTA has two identical branches for the CMFB loop. The dominant pole is  $g_{oc}/C_c$ , and the non-dominant poles are located at  $g_{m4}/C_B$  and  $g_{m8}/C_A$ . For a load capacitor  $C_L = 0.9$  pF, the simulated CMFB open-loop phase margin of the integrator is  $68^\circ$  at the unity-gain frequency of 160 MHz.

IV. FILTER ARCHITECTURE AND AUTOMATIC TUNING SYSTEM

The equiripple linear phase filter architecture is shown in Fig. 4. The same transconductance is used for all of the six  $G_m$  cells. Scaled transconductances are used for  $G_{mQ1}$  and  $G_{mQ2}$  in order to adjust the *Q*s of the biquads. Two complete CM control circuits have been used to control the two outputs *B* and *D*. As a result of the pseudodifferential structure used, *A* and *C* are low-impedance nodes for both differential signals and common-mode signals; hence, we only use Part A of the CM control circuit (Fig. 2) to provide CMFF and adaptive bias for these nodes.

A simple automatic frequency-tuning system is used to compensate the variations of the pole locations. The topology is based on the architecture reported in [8]; the principle of the automatic tuning system is shown in Fig. 5. The OTA  $G_m$  is a replica of the transconductor used in the filter and is used as a part of an integrator. By comparing the magnitude of the reference input signal with the integrator's output signal, we can tune the integrator's unity-gain frequency to the desired value.

V. EXPERIMENTAL RESULTS

The proposed OTA and the filter have been fabricated in a 0.35- $\mu$ m CMOS process through the MOSIS service. The chip micrograph is shown in Fig. 6. With a single 2.3-V power supply, experimental results show that the OTA and the filter's THD are  $-48$  and  $-44$  dB for a  $2-V_{pp}$  differential input at

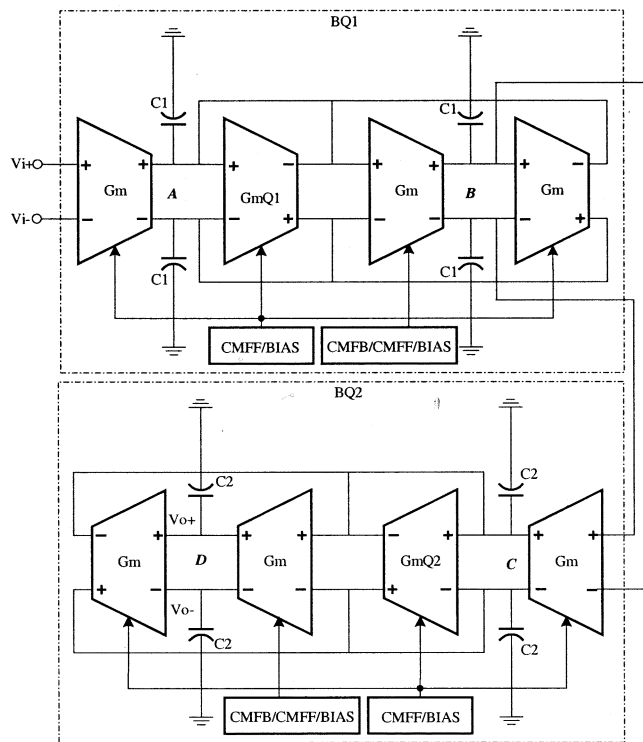


Fig. 4. Fourth-order equiripple linear phase filter.

20 MHz, respectively. The third-order intermodulation (IM3) of the filter for a two-tone input signal of 1  $V_{pp}$  each (at 60 and 70 MHz) is  $-40$  dB, as shown in Fig. 7. The measured inband IM3 is shown in Fig. 8; notice that the IM3 is less than  $-38$  dB over the whole filter bandwidth. For the filter tuned at 150 MHz, the filter's group delay response is shown in Fig. 9. The filter's group delay ripple is less than  $\pm 100$  ps up to  $1.5 f_c$ , as expected. The magnitude response of the filter, driven by

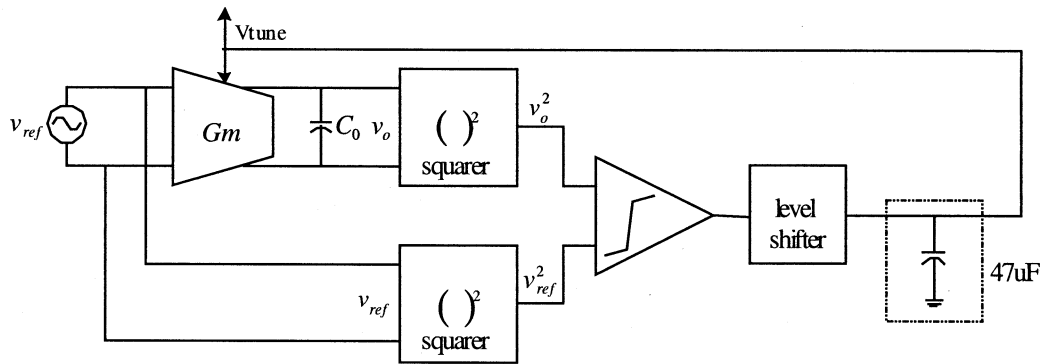


Fig. 5. Block diagram of the automatic tuning system.

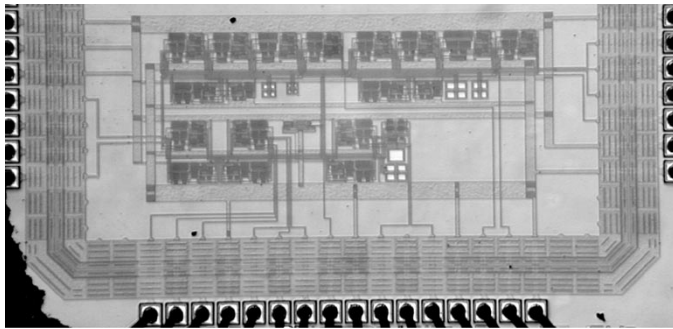


Fig. 6. Chip micrograph.

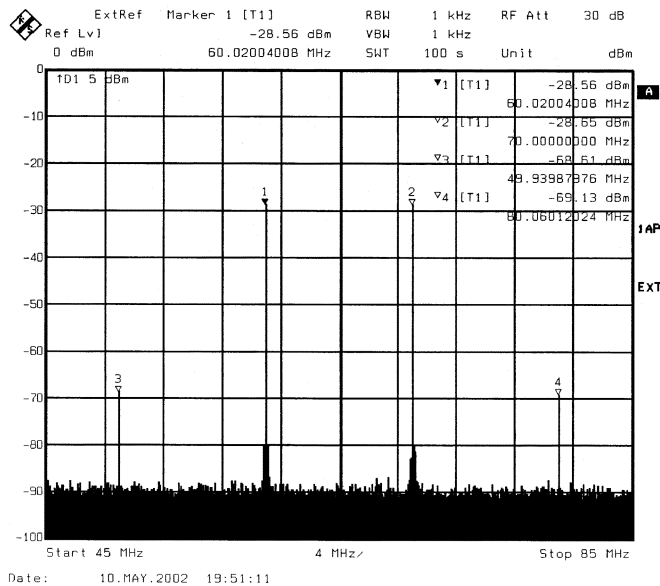


Fig. 7. Filter's IM3 for a two-tone input (at 60 and 70 MHz) of 1 V<sub>pp</sub> each.

the automatic tuning system, is shown in Fig. 10. The filter dynamic range is 52 dB at THD < -44 dB, and the power consumption of the whole system is 90 mW. The measured performances of the filter are summarized in Table I. The experimental results of this work are compared with previous realizations [9]–[12] in Table II. Notice that our topology does not include gain-boosting techniques and the others do not have automatic tuning systems. With the cheaper technology and the

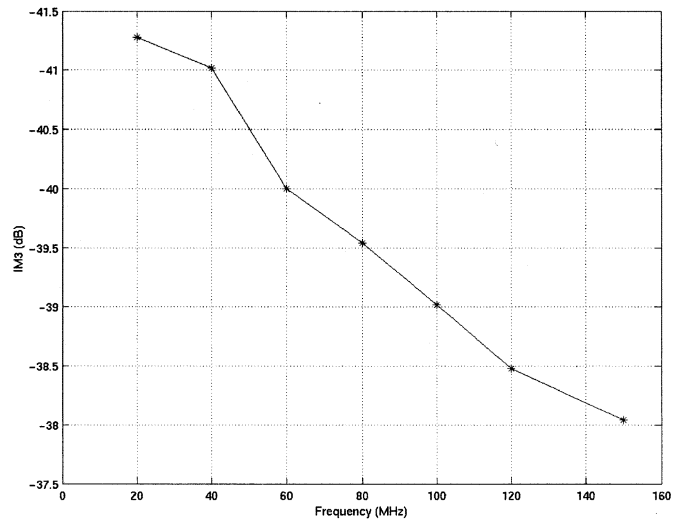


Fig. 8. Filter's IM3 versus frequency ( $V_1 = 1 V_{pp}$ ,  $V_2 = 1 V_{pp}$ ).

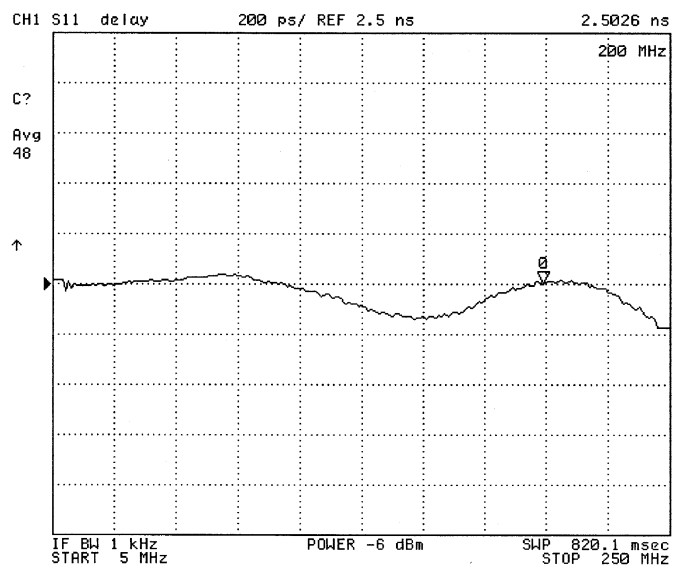


Fig. 9. Filter's group delay response with a bandwidth of 150 MHz.

lowest power-supply voltage, the proposed filter has the largest linear signal swing.

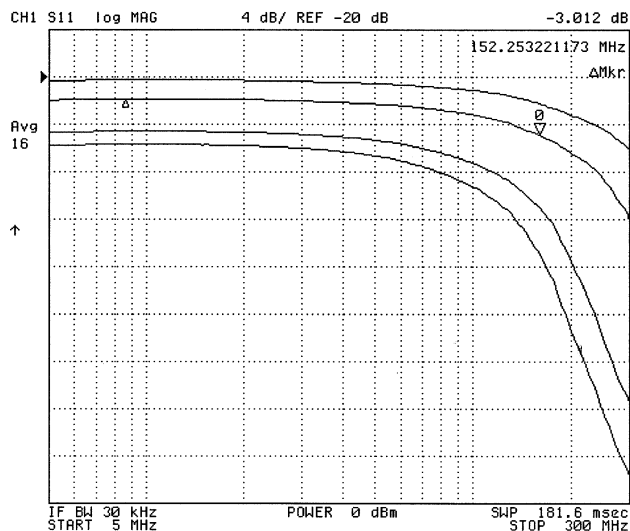


Fig. 10. Filter’s magnitude response with automatic frequency tuning system ( $f_{-3\text{ dB}} = 80, 100, 150,$  and  $200\text{ MHz}$ ). DC gain changes because the output buffer (another OTA) is driven by the automatic tuning system as well.

TABLE I  
PERFORMANCE SUMMARY OF THE STANDALONE FILTER PROTOTYPE  
FABRICATED IN CMOS  $0.35\ \mu\text{m}$

Process	0.35um CMOS
Filter type	4 <sup>th</sup> -order equiripple
Power supply	2.3V
Power consumption	72mW
Cutoff frequency	80-200MHz
Group delay ripple	<4% up to $1.5f_c$
Noise level ( $BW=150\text{MHz}$ )	1.69mV <sub>rms</sub>
Differential input for THD<-44dB @20MHz	2V <sub>pp</sub>
Dynamic range @THD=-44dB	52dB
Worst case CMRR @f=150MHz	32dB
Worst case PSRR <sup>+</sup> @f=150MHz	21dB
Worst case PSRR <sup>-</sup> @f=150MHz	22dB

TABLE II  
COMPARISON OF SEVERAL LINEAR PHASE FILTERS

Parameters	[9]*	[10]*	[11]*	[12]*	This work
$f_c(\text{MHz})$	10-100	30-100	30-120	80-200	80-200
Technology	0.29um BiCMOS	0.25um CMOS	0.25um CMOS	0.25um CMOS	0.35um CMOS
$V_{in,max}(mV_{pp})$	100	200	200	800	2000
THD @ $V_{in,max}(dB)$	-46	-46	-50	-42	-44
Dynamic Range(dB)	40	--	45	--	52
Power/Pole (mW)	17	30	15	30	22
Supply Voltage(V)	3	2.5	2.5	3	2.3

## VI. CONCLUSION

The optimal design of a pseudodifferential transconductor using transistors operating in triode region has been discussed. A CM control circuit that combines CMFB, CMFF, and adaptive bias has been presented. A large linear signal swing has been achieved due to the well-controlled CM behavior. The principle of the CM control circuit can be easily applied to the design of fully differential structures, and it is well suited for low-voltage pseudodifferential architectures.

Experimental results of both the OTA and the 80–200-MHz fourth-order linear phase filter are in good agreement with the theoretical results. The ratio of the root mean square value of the ac signal to the power supply voltage is around 31%, which is much better than previous realizations.

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