

Low-Voltage High-Speed Switched-Capacitor Circuits Without Voltage Bootstrapper

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Abstract—Low-voltage high-speed switched-capacitor (SC) circuit design without using voltage bootstrapper is presented. The basic building block used for low-voltage SC circuit design is the auto-zeroed integrator (AZI), which can work at both low voltage and high sampling frequency. With this method, two low-voltage SC systems were successfully designed and implemented in 1.2- μm CMOS technology. The first one is a fully differential SC bandpass biquad working at 1.5 V and 5.0-MHz clock frequency. The measured Q value is 8.0 at the center frequency of 833 kHz. The second one is a fully differential fourth-order bandpass $\Delta\Sigma$ modulator that also works at 1.5 V and 5.0 MHz. Its measured third-order intermodulation is less than -78 dBc due to the low distortion characteristic of AZI. The measured signal-to-noise ratio of the modulator is 61 dB within the narrow band of 25 kHz centered at 1.25 MHz.

Index Terms—Bandpass delta-sigma modulator, high-speed switched-capacitor circuits, low-voltage switched capacitor, switched-capacitor bandpass filter.

I. INTRODUCTION

A WELL-KNOWN difficulty of low-voltage switched-capacitor (SC) circuit design is that the gate-driving voltage V_{GS} of the input CMOS switch is not large enough. Currently, there are two major approaches for low-voltage SC design using standard CMOS technologies. The first one is to add an on-chip voltage bootstrapper and generate higher clock voltages to drive switch gates only, while other circuits are unchanged [1], [2]. However, the existence of on-chip high voltages is a danger for deep-submicrometer CMOS processes. The second method is switched-opamp technology. The opamp in the integrator is turned on and off to transfer voltage signals to the next integrator stage, so no input switch is required to sample the input voltage [3]–[6]. It is a real low-voltage SC circuit, but it is not suitable for high-speed SC circuit applications because turning opamps on/off needs much more time than turning switches on/off.

The auto-zeroed integrator (AZI) was originally used for offset cancellation in SC circuits [7]. Its application for low-voltage SC circuits was reported in [8]. Here, AZI was modified for the design of low-voltage and high-speed SC without bootstrapped clock voltage. Although circuits using a similar prototype were found recently [9], [10], this brief demonstrates an independent research having different design purposes and tradeoffs (also presented at a conference [11]).

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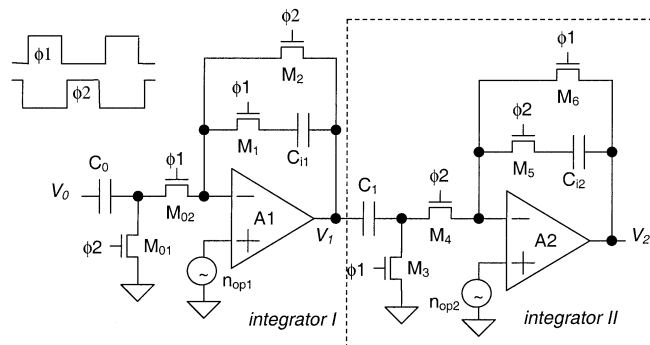


Fig. 1. Single-ended schematics of AZI. $\phi 1$ and $\phi 2$ are nonoverlap clock phases.

There are differences between the methods used in this brief and the techniques in [9] and [10].

- 1) This AZI is designed to work at both high speed and low voltage.
- 2) The AZI has a fully differential structure.
- 3) There is no forward biasing of the p-n junctions of switches (a common problem for low-voltage SC design [4]).

In Section II, an AZI is analyzed to explain why it can be used as the basic building block of low-voltage high-speed SC circuits. In Section III, a 1.5-V 5-MHz fully differential SC bandpass biquad is designed using AZI. Section IV shows a 1.5-V 5-MHz fully differential fourth-order bandpass $\Delta\Sigma$ modulator. Its center frequency locates at 1/4 of the sampling frequency. Both circuits were fabricated in 1.2- μm CMOS process and their characterization results are listed. A final summary and discussion follows in Section V.

II. AUTO-ZEROED INTEGRATOR

In an AZI, the charge is transferred by switching the integrating capacitor of the previous integrator, not by switching the opamp as in a switched-opamp integrator. Two continuously connected AZIs are shown in Fig. 1 (one side of the fully differential structure). C_1 is charged to V_1 by Integrator I after M_1 is closed in $\phi 1$. At the same time, Integrator II is in the reset phase since M_6 is closed, but the charge stored in C_{i2} is not lost because M_5 is open. In $\phi 2$, M_1 is turned off and the output of Integrator I is reset to zero. As a result, the charge in C_1 is dumped to C_{i2} in Integrator II. The stored charge in C_{i1} is not lost during the reset phase of $\phi 2$. Consequently, the charge is transferred from Integrator I to Integrator II. If Integrator II is

isolated for the convenience of analysis, the transfer function is expressed as a half-delay integrator.

$$H(Z) = \frac{V_2}{V_1} = \frac{C_1}{C_{i2}} \frac{Z^{-\frac{1}{2}}}{1 - Z^{-1}}. \quad (1)$$

It is important to notice that all switches in Fig. 1 are nMOS transistors whose sources are connected to the common-mode voltage V_{CM} and gates are connected to the supply voltage V_{DD} , which is expressed as $V_{GS} = V_{DD} - V_{CM}$. This means that V_{GS} is not signal dependent. If we assume that $V_{CM} \approx 0.5$ V to keep a reasonable output swing range and $V_{TH} \approx 0.8$ V to satisfy the requirement of $V_{GS} > V_{TH}$ to turn on a switch, the supply voltage should be $V_{DD} > V_{TH} + V_{CM} \approx 1.3$ V. This explains why AZI can work at 1.5 V in 1.2- μm CMOS. It also reveals that it is hard to lower the supply voltages further because of the existence of V_{CM} . Since the voltage swing is limited to be less than V_{CM} , the forward biasing of the p-n junction of nMOS switch is avoided.

The time needed to auto-zero the output of Integrator I or Integrator II is usually much shorter than the time used to charge C_{i1} or C_{i2} , because not only is the integrating capacitor larger than the input capacitor in most cases, but there is also the feedback factor. As a result, the settling of AZI is dominated by the settling time of the integrator (the opamp bandwidth and feedback factor), which is similar to the settling of the output voltage in a conventional SC integrator. This fact indicates that low-voltage AZI can work at clock speeds very close to the speed of a conventional SC circuit. Moreover, the working conditions (voltage and current biases) of the opamp are not disturbed during operations. This makes AZI more suitable than switched-opamp circuits for the design of high-speed SC circuits.

Because the channel voltages of the nMOS switch are fixed at V_{CM} , there is no signal-dependent switch channel voltage, and therefore no signal-dependent charge injections. It is clear that there is no need to use the delayed clock phases as used in conventional SC circuits. For the same reason, the on-resistance of all switches is not related to the signal level. So, AZI does not have these two major sources of distortion appearing in conventional SC circuits.

Fig. 2 shows the basic schematics of a two-stage fully differential opamp used in 1.5-V AZI. The main opamp is composed of $M_0 \sim M_8$. The common-mode feedback (CMFB) circuit is formed by $M_9 \sim M_{12}$. This opamp has a unique dynamic common-mode detection circuit ($C_1 \sim C_4$) working at 1.5 V without any signal-dependent switch. The detected common-mode voltage is compared to V_{CM} through M_9 and M_{10} . The result is fed back to the input stage of the opamp through a current mirror. Both C_1 and C_2 are discharged in ϕ_1 (the integrating phase) because both $out+$ and $out-$ are auto-zeroed by the integrator. In ϕ_2 , output voltages are sampled by C_1 and C_2 and integrated with C_3 and C_4 . These four capacitors and the switch perform as an RC voltage divider.

III. FULLY DIFFERENTIAL BANDPASS FILTER

Using AZI as the basic building block, a fully differential second-order bandpass SC filter was designed. The sampling frequency is $F_S = 5.0$ MHz at 1.5 V. The center frequency is

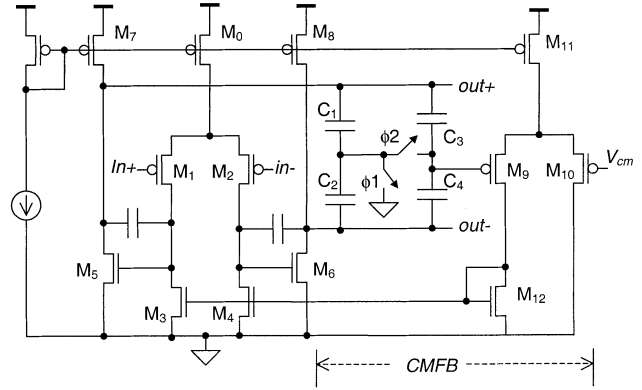


Fig. 2. Simplified schematic of a low-voltage two-stage differential opamp with dynamic CMFB.

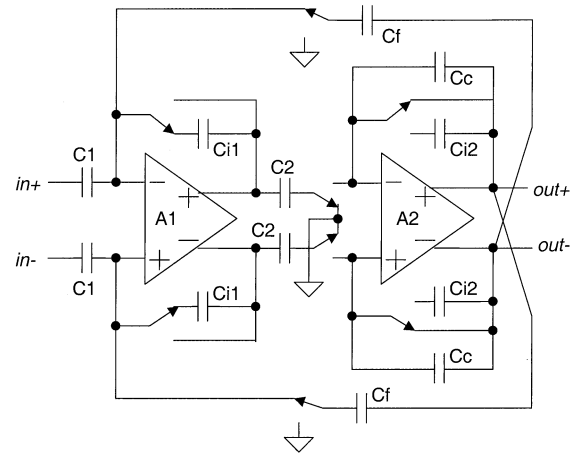


Fig. 3. Schematic of a fully differential second-order bandpass filter using AZI. The positions of switches are in ϕ_1 .

designed at $F_C = F_S/6 = 833.33$ kHz. A simplified schematic is shown in Fig. 3, which is composed of two stages. The first stage is an AZI that has been well described in Fig. 1. The capacitor-coupled input provides rail-to-rail input common-mode voltages and adds a factor of $1 - Z^{-1/2}$. The second stage is a “lossy” AZI, where the charge in C_C is discharged during the reset, with the transfer function of

$$H_{i2}(Z) = \left(\frac{C_2}{C_{i2} + C_C} \right) \frac{Z^{-\frac{1}{2}}}{1 - \alpha Z^{-1}} \quad (2)$$

where $\alpha = C_{i2}/(C_{i2} + C_C)$. Capacitor values are $C_1 = 0.5$ pF, $C_2 = 2.31$ pF, $C_{i1} = 1.95$ pF, $C_{i2} = 2.15$ pF, $C_C = 0.3$ pF, and $C_f = 1.92$ pF. The z-domain transfer function of the SC biquad is

$$H_{\text{biquad}}(Z) = \frac{V_{\text{out}}(Z)}{V_{\text{in}}(Z)} = \frac{0.2418 (Z^{-1} - Z^{-\frac{1}{2}})}{1 - 0.9492Z^{-1} + 0.8776Z^{-2}}. \quad (3)$$

For $V_{CM} = 0.45$ V and $V_{DD} = 1.5$ V, the gate voltage of any nMOS switch is 1.5 V $-$ 0.45 V $=$ 1.05 V. Because there is no signal-dependent switch and no pMOS switch, only a single clock phase is needed. Hence, the SC filter has a more compact structure and reliable performance.

TABLE I
TESTING RESULTS OF THE SC BANDPASS BIQUAD USING AZI

Parameter	Value	Unit	Note
Clock frequency (F_S)	5.0	MHz	
Power supply voltage (V_{DD})	1.5	V	
Common mode voltage (V_{CM})	0.45	V	
Input common mode Voltage	0~1.5	V	Rail-to-rail
Differential input voltage (V_{in})	0.5	V _p	Peak value
Center frequency (F_C)	823.1	KHz	
Output swing range	0.5	V _p	Peak value
Q-factor	8.0		
Biasing current	740	μ A	
Die size	1.12	mm ²	1.2 μ m process

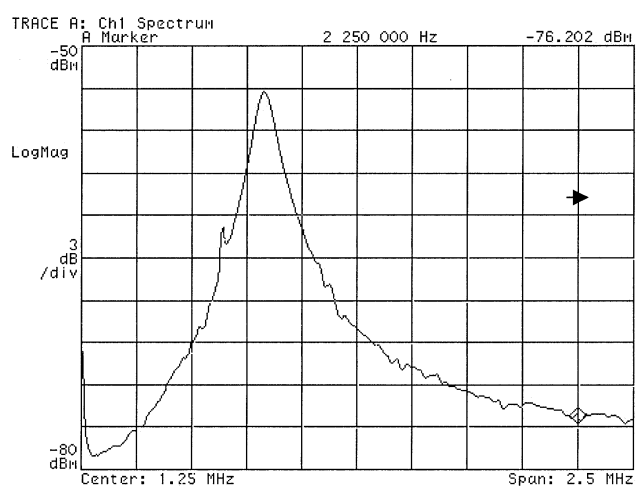


Fig. 4. Plot of the magnitude response of the second-order bandpass filter at $F_S = 5.0$ MHz.

The test circuit in Fig. 3 was fabricated in MOSIS double-metal double-poly 1.2- μ m CMOS process. The capacitors were realized with a 0.1-pF poly1-poly2 unit capacitor. Some of the important testing data are listed in Table I. The measured center frequency value is 823.1 kHz, which is -1.2% off from the designed value. Fig. 4 is a plot of the magnitude response of the SC bandpass filter at $F_S = 5.0$ MHz. The glitch appearing on the curve is just a plotting artifact that did not appear when the actual output waveform was observed. Fig. 5 is a copy of an oscilloscope waveform of the filter output voltage (fully differential was converted to singled-ended). It is obvious that there is no sign of the settling uncertainty in the waveform.

IV. FULLY DIFFERENTIAL FOURTH-ORDER BANDPASS $\Delta\Sigma$ MODULATOR

The second test circuit of the low-voltage SC circuits using AZI is a fourth-order fully differential bandpass $\Delta\Sigma$ modu-

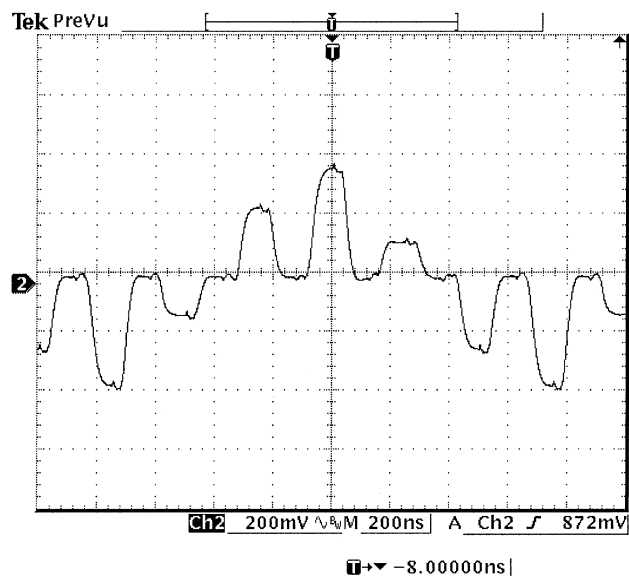


Fig. 5. Waveform of the output voltage of the bandpass filter. The differential output voltage was converted to a single-ended voltage and buffered.

lator with a 1-bit quantizer. The sampling rate F_S is 5.0 MHz and bandwidth is 25 kHz centered at $F_C = 1.25$ MHz ($1/4$ of F_S). It is composed of two stages of resonators built with AZI. Fig. 6 shows the system diagram of the modulator. Because AZI has only a half-clock delay, half-delay units have to be added in feedback paths to keep the loop transfer function correct. V_{out} is the 1-bit output data. $H(Z)$ denotes an AZI whose transfer function is $Z^{-1/2}/(1-Z^{-1})$. The capacitor coupling input is represented by $d(Z) = 1 - Z^{-1/2}$. Other coefficients are $a_1 = 0.1156$, $a_2 = 1.802$, $a_3 = 0.315$, $a_4 = 1.518$, $b_1 = 0.11$, $b_2 = 0.19$, $b_3 = 0.108$, $r_1 = 1.096$, and $r_2 = 1.329$. N_Q represents the quantization noise. By using resonators to build the modulator, the poles of the transfer function are located on the unit circle such that any mismatch does not allow poles to leave the unit circle [13]. Therefore, the quantization noise attenuation is less sensitive to coefficient variations. Linear approximations of the signal and noise transfer functions [12] are as shown in (4a) and (4b) at the bottom of the page.

Fig. 7 is the fully differential SC schematic of Fig. 6. Opamps $A1 \sim A4$ are illustrated in Fig. 2. The analog comparator $A5$ is similar to that reported in other low-voltage SC papers [5]. $V_{ref} = 1.4$ V, $C_{a1} = 229$ fF, $C_{a2} = 2.0$ pF, $C_{a3} = 555$ fF, $C_{a4} = 838$ fF, $C_{i1} = 1.98$ pF, $C_{i2} = 1.11$ pF, $C_{i3} = 1.76$ pF, $C_{i4} = 552$ fF, $C_{r1} = 2.17$ pF, $C_{r2} = 2.34$ pF, $C_{b1} = 217$ fF, $C_{b2} = 210$ fF, and $C_{b3} = 191$ fF. All switches are nMOS transistors, except the pMOS switches connected to the reference

$$H_S(Z) = \frac{V_{out}}{V_{in}} = \frac{0.0996Z^{-2} (Z^{-\frac{1}{2}} - Z^{-1})}{1 - 0.0076Z^{-1} + 1.7448Z^{-2} - 0.0074Z^{-3} + 0.8361Z^{-4}} \quad (4a)$$

$$H_N(Z) = \frac{V_{out}}{N_Q} = \frac{1 - 0.0076Z^{-1} + 1.9996Z^{-2} - 0.0076Z^{-3} + Z^{-4}}{1 - 0.0076Z^{-1} + 1.7448Z^{-2} - 0.0074Z^{-3} + 0.8361Z^{-4}} \quad (4b)$$

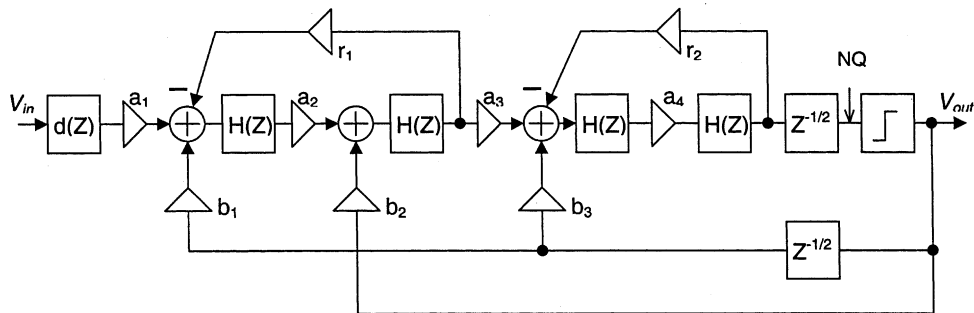


Fig. 6. Block diagram of the fourth-order bandpass delta-sigma modulator using AZI.

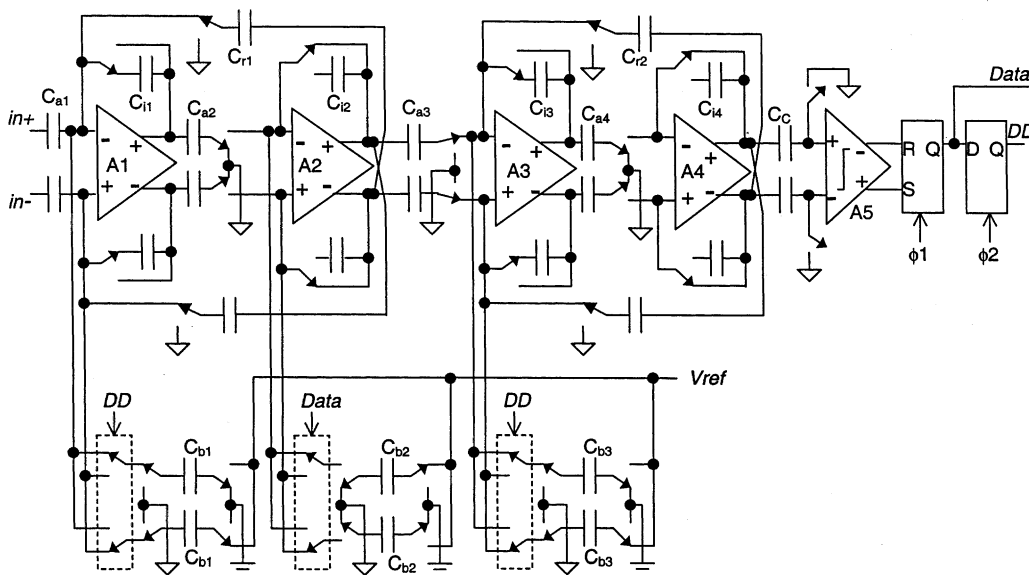


Fig. 7. Schematics of the fully differential SC fourth-order bandpass $\Delta\Sigma$ modulator. The output is the 1-bit *Data*. Positions of switches are in $\phi 1$. Positions of feedback switches (controlled by *Data* or *DD*) are at the state of 1.

TABLE II
TESTING RESULTS OF FOURTH-ORDER SC BANDPASS MODULATOR USING AZI

Parameter	Value	Unit	Note
Clock frequency (F_s)	5.0	MHz	
Central frequency (F_C)	1.25	MHz	One-fourth of F_s
Signal bandwidth	25	KHz	OSR = 100
Power supply voltage (V_{DD})	1.5	V	
Common mode voltage (V_{CM})	0.45	V	
Input common mode voltage	0~1.5	V	Rail-to-tail
Differential input voltage (V_{in})	1.1	V _p	Full scale peak value
Power dissipation	2.6	mW	
Die size	1.53	mm ²	1.2 μ m process
Signal-to-noise ratio (SNR)	61	dB	
Third order inter-modulation (IM3)	<-78	dBc	-6dB twin-tones near F_C

voltage of V_{ref} . As mentioned in Section II, there is no need to use delayed clock signals to reduce charge injections.

This test circuit was also implemented in MOSIS 1.2- μ m CMOS technology. Important testing data are listed in Table II. The 1-bit data output was collected with a logic analyzer. The total record length was around 32 000 bits. For a twin-tone input 6-dB below the full-scale input amplitude near F_C , the third-order intermodulation (IM3) can be estimated in Fig. 8. It matches the low-distortion characteristic of AZI because of no

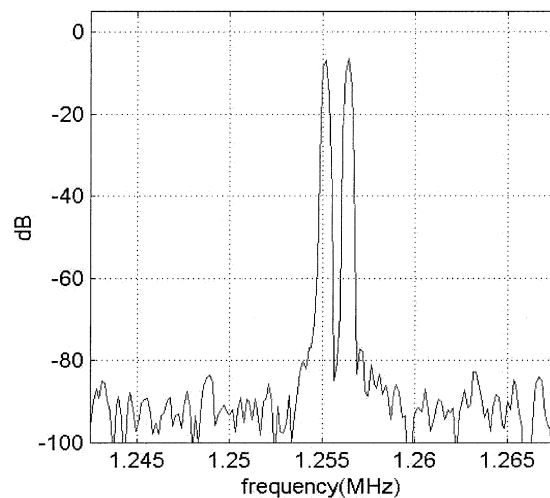


Fig. 8. Twin-tone testing results near F_C . The signal level is half of the full scale.

signal dependence. The noise performance was mostly limited by capacitor sizes and parameter values of the first-stage resonator. Less thermal noise can be achieved by increasing capacitor sizes and the opamp power. Fig. 9 is a plot of the

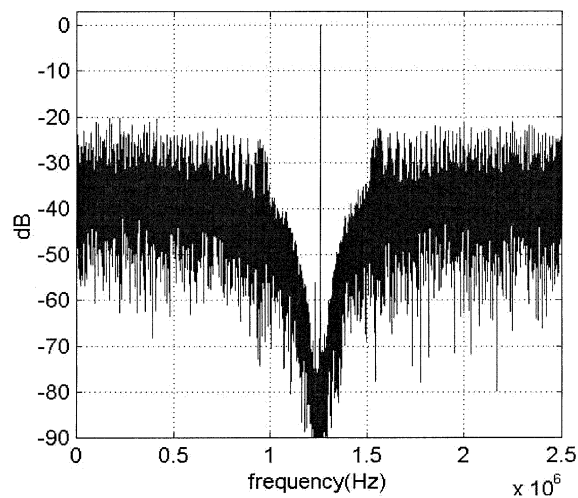


Fig. 9. Noise-shaping spectrum of the 1-bit data output of the bandpass delta-sigma modulator.

magnitude response of the 1-bit output from 0 to $F_S/2$ for a full-scale input voltage.

V. CONCLUSION

Both a fully differential SC bandpass biquad and a fourth-order bandpass $\Delta\Sigma$ modulator circuit using AZI at 1.5 V were successfully designed. There is no need for internal voltage bootstrapper. The clock speed of AZI is near that of conventional SC circuits. Low distortion is observed because there are no signal-dependent switches. For this reason, delayed clock phases are no longer needed. There is no forward biasing of p-n junctions of nMOS switches, so no extra circuits are needed to prevent the forward biasing from happening. As the tradeoff of pursuing both high speed and low voltage, as well as a more conventional structure, the supply voltage cannot be aggressively lowered to around 1.0 V in these circuits.

Low-voltage SC circuits using AZI could find applications in broad-band and wireless communications such as the Bluetooth system.

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