

A Wide Input Bandwidth 7-bit 300-MSample/s Folding and Current-Mode Interpolating ADC

Yunchu Li, *Member, IEEE*, and Edgar Sánchez-Sinencio, *Fellow, IEEE*

Abstract—A 7-bit Nyquist folding and interpolating analog-to-digital converter (ADC) that converts at 300 MSamples/s is presented. Using current-mode signal processing techniques for analog preprocessing and a front-end sample-and-hold, the proposed 7-bit folding and interpolating ADC yields a wide input bandwidth up to 60 MHz with six effective number of bits. The ADC consumes 200 mW from a 3.3-V power supply. The chip occupies 1.2 mm² active area, fabricated in 0.35- μ m CMOS.

Index Terms—Current comparator, current-mode interpolation, folding and interpolating analog-to-digital converter (ADC), OTA-based folder, time interleaving sample-and-hold.

I. INTRODUCTION

HIGH-SPEED analog-to-digital converters (ADCs) are key elements in the read channel of optical and magnetic data storage systems. The required resolution is low (6–7 bits), while the sampling rate and effective resolution bandwidth requirements increase with each generation of storage system. For example, a 16 \times DVD system demands a 7-bit 432-MSamples/s ADC [1]. Such an ADC should exhibit low latency and good linearity.

Folding and interpolating (F&I) ADCs have been shown to be an effective means of digitizing high-bandwidth signals at low-to-medium resolution with high sample rate. Although CMOS technology is less suitable for this architecture because of lower transconductance and relatively modest device matching, F&I ADCs with sample rates as high as 400 MSamples/s (6 bit) have been reported [2]–[8], but unfortunately some converters' bandwidths [3]–[6] are much smaller than Nyquist bandwidth.

In this brief, we analyze the bandwidth in F&I ADCs and propose solutions to obtain larger bandwidth. Section II describes the basic F&I ADC architecture and the nonidealities that limit its performance. Section III details the implementation of building blocks of the proposed F&I ADC, and Section IV presents the experimental results. Conclusions are presented in Section V.

II. FOLDING PRINCIPLE

The main motivation for an F&I ADC in comparison with a flash ADC was the dramatic reduction of the number of comparators required in the design. In a full-flash ADC architecture,

Manuscript received September 27, 2002; revised March 18, 2003.

Y Li was with the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843 USA. He is now with Analog Devices Inc., Wilmington, MA 01887 USA.

E. Sánchez-Sinencio is with the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843 USA (e-mail: sanchez@ee.tamu.edu).

Digital Object Identifier 10.1109/JSSC.2003.814429

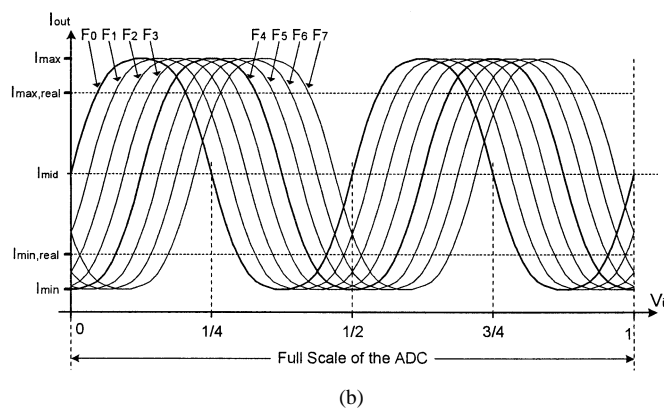
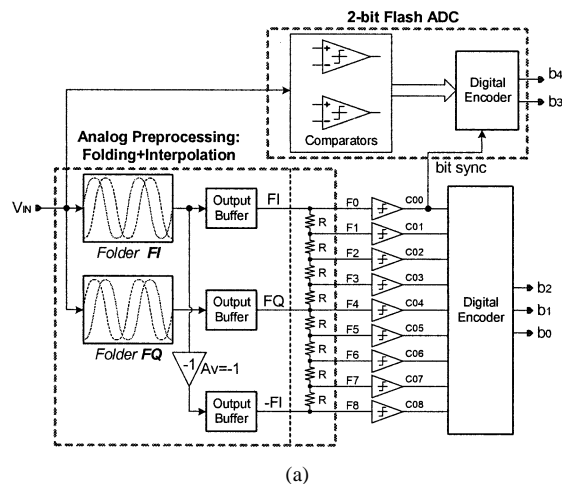


Fig. 1. Conventional implementation of 5-bit F&I ADC. (a) Simple schematic. (b) Folding waveforms to show how 32 zero crossing points are generated. ($N_P = 2$, $F_F = 4$, $F_I = 4$.)

$2^N - 1$ comparators are required for an N -bit converter. This is often the largest part of such a chip in power, device count, and area. The analog folding architecture allows each comparator to detect more than one zero-crossing points; the number of zero crossings is referred to as the folding factor, and it reduces the number of comparators by nearly the same factor. A simple block diagram of a 5-bit folding ADC and its folding waveforms is depicted in Fig. 1. In this case, each comparator can detect four zero-crossing points. A 2-bit coarse quantizer is required to determine two MSBs since the folding transfer characteristics are periodic. In this example, the 5-bit F&I ADC uses 12 comparators whereas a full-flash 5-bit ADC would require 31 comparators.

Interpolation is often employed to generate extra folding waveforms. A folding ADC utilizing interpolation is usually called an F&I ADC. The 5-bit F&I ADC shown in Fig. 1 uses eight resistors to implement two 4 \times interpolators. Resolution N_B of an F&I ADC is related to the number of primary folding

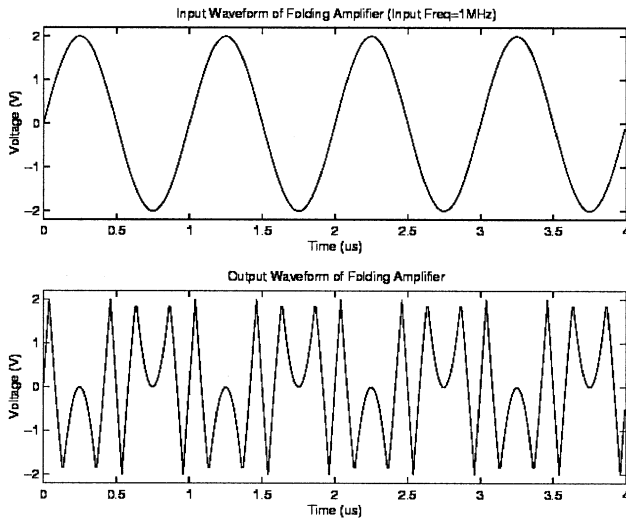


Fig. 2. Frequency multiplication effect (upper trace is input signal, lower trace is output of folder).

waveforms N_P , folding factor F_F , and interpolation factor F_I by

$$N_B = \log_2(N_P \cdot F_F \cdot F_I) \quad (1)$$

For a given resolution, the choice of N_P , F_F , and F_I usually involves tradeoffs among resolution, bandwidth, and cost. For the 7-bit F&I ADC, we choose $N_P = 4$, $F_F = 4$, and $F_I = 8$ based on behavioral simulation results.

A. Frequency Multiplication Effect

The frequency multiplication effect is inherent to folding ADCs due to the “folding” transfer characteristic of folders. As shown in Fig. 2, a $4\times$ folder converts a 1-MHz full-swing continuous-time sinusoid input to a higher frequency signal. Thus, the folder and interpolator must have much higher bandwidths or the ADC performance will suffer. The frequency multiplication effect is proportional to the folding factor F_F and also depends on input signal amplitude.

We use a front-end sample-and-hold (S/H) block to alleviate this problem. For a discrete-time system with sample rate f_s , the signal frequency cannot exceed Nyquist frequency ($f_s/2$). Behavioral models are constructed to analyze the impact of frequency multiplication on 7-bit 300-MSamples/s F&I ADCs with/without front-end S/H. We fix the folder’s bandwidth at 300 MHz and sweep the input frequency from dc to Nyquist rate. The behavioral simulation results of four cases, with and without S/H, are compared in Fig. 3. The 3-dB bandwidths of F&I ADCs with $4\times$ and $8\times$ folders without S/H are 42 and 27 MHz, respectively. As shown in the two upper traces in Fig. 3, the F&I ADCs with S/H maintain much better performances even at Nyquist rate.

B. Voltage-Mode and Current-Mode Interpolation

Ideally, an interpolator should generate equidistant zero crossing points. Resistor interpolators are used in most conventional F&I ADCs. In a resistor-based voltage-mode interpolating system, the interpolation accuracy is limited by

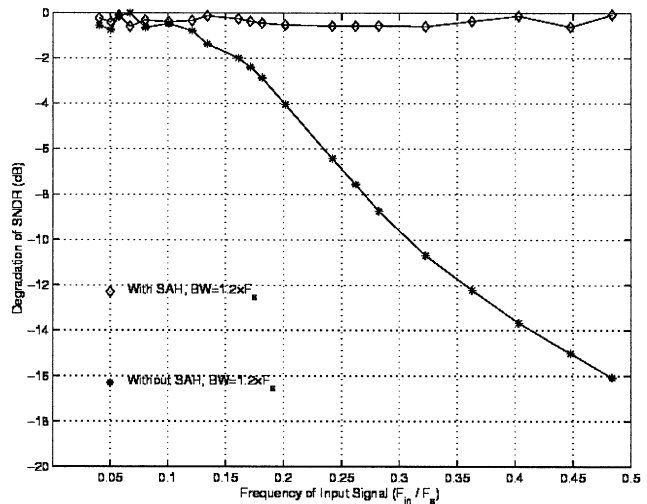


Fig. 3. SNDR degradation versus input signal frequency on 7-bit F&I ADCs with and without front-end S/H.

resistor mismatch. Care should be taken to ensure that the RC constant formed by these resistors and the input capacitances of comparators and parasitic capacitance does not limit the system sample rate. To drive the low impedance interpolating resistor ladder, wide-band low output impedance buffers must be used between folders and interpolators. In many designs [5], source followers are used to implement the buffer, which has very limited voltage swing with low power supply voltages, however, a large voltage swing is essential to yield an acceptable signal-to-noise ratio (SNR).

Current-mode interpolators [2], [9], in which signals are represented by current swings, are more suitable for low-voltage design. Strictly speaking, the current-mode interpolator in [2] should be called “transconductance-mode” interpolation, because the input signal of the interpolator is a voltage signal. Thus, it still has a voltage swing problem at the output of the voltage-mode folder.

We propose a different approach to implement true current-mode analog preprocessing which combines an operational transconductance amplifier (OTA)-based folder with a current-mirror-based interpolator to alleviate voltage swing difficulties. As shown in Fig. 4, the signal processing of folding and interpolation are both carried out in current mode. A system block diagram of our proposed architecture is illustrated in Fig. 5. Here, four folders are used in our system to reduce the interpolation error caused by nonlinear “pseudosinusoid” folder transfer characteristics. The aforementioned S/H block precedes the F&I ADC to alleviate the frequency multiplication effect and boost the dynamic performance. Current-mode signal processing is used in the fine quantizer path to reduce voltage swings and achieve high speed.

III. CIRCUIT DESCRIPTION

In this section, we describe the ADC architecture and introduce its building blocks. The actual ADC is fully differential but, for the sake of brevity, most blocks are illustrated in single-ended form. The block diagram of the proposed F&I ADC is shown in Fig. 5.

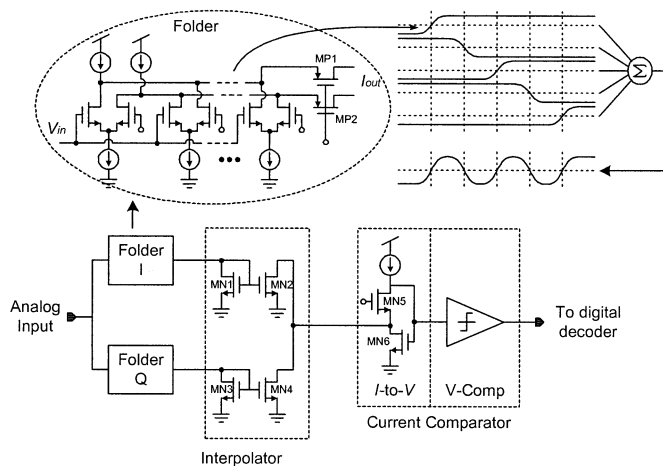


Fig. 4. Simplified schematic of the current-mode analog preprocessing in the fine quantizer channel.

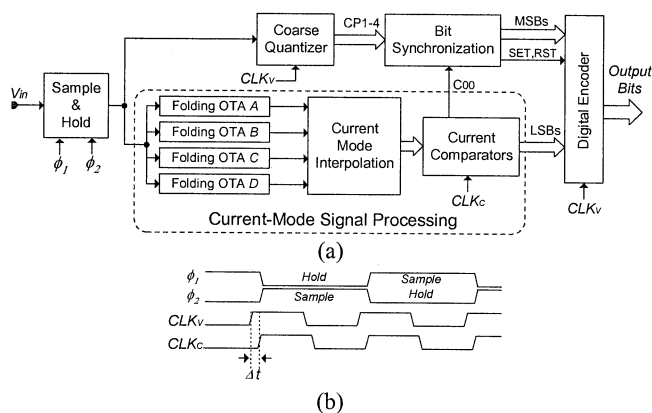


Fig. 5. Proposed current-mode F&I ADC. (a) Block diagram. (b) Clock waveforms. (Δt is used to compensate the delay difference, which is caused by analog preprocessing, between coarse and fine paths.)

The analog input signal is sampled by the S/H unit, which feeds four OTA-based folders yielding four primary folding currents. Current-mirror-based interpolators generate 32 folding currents, from which 128 (7-bit) zero-crossing points are detected by 32 comparators. The 32-bit code produced by the comparators is called a cyclic thermometer code, which can be easily encoded into a 5-bit binary code. The five LSBs are combined with the two MSBs from the coarse quantizer to form the 7-bit output of the F&I ADC.

A. Time-Interleaved Sample-and-Hold

The requirement on the S/H in an F&I ADC is no different when compared with a flash ADC. The only exception is that the S/H used in an F&I ADC must settle faster, because the S/H must leave time for the analog preprocessing units to fully settle. For this reason, we chose the time-interleaved structure similar to the S/H in [11]. Each path of the time-interleaved structure has the same circuit structure as the one used in [12]. A potential problem with interleaving is the mismatch (timing, gain, offset) between the two channels. Any timing mismatch or gain mismatch results in an intermodulation between the input frequency and half the sampling frequency. Any offset mismatch results in a tone at half the sampling frequency (Nyquist tone). We as-

sume the Nyquist tone can be suppressed by digital equalization circuitry following the F&I ADC [11]. Clock edge realignment circuitry is used to suppress timing mismatches in the two interleaving paths.

B. Folded Cascode OTA-Based Folder

Different implementations of producing folding signals have been proposed since F&I ADC was first introduced, but the most popular method involves the use of differential pairs [2]–[8]. In all above cases, the outputs of differential pairs are connected to the relatively high impedance loads, while in our design the loads are common-gate amplifiers with low input impedance, as shown in Fig. 4. This is the difference between voltage-mode and current- (or transconductance-) mode circuits. Current-mode circuits are usually considered more suitable for low-supply-voltage design because signals are represented by current swings, and they usually have very wide bandwidth, but accuracy is not as high as that of closed-loop voltage-mode circuits.

Five differential pairs are used to construct a $4\times$ folder. When the input voltage is swept from the lower to upper limit of the ADC input full scale, the differential pairs DP1, DP3, DP5 will generate positive slopes and differential pairs DP2 and DP4 will generate negative slopes. The combination of all five output currents produces a pseudosinusoidal folding transfer characteristic. A PMOS common-gate amplifier is used as a current buffer to reduce the loading effect at the current summation nodes. By adjusting the value of the five reference voltages connected to these five differential pairs, we can obtain different folding transfer characteristic curves with different phase, such as F_0 and F_4 as illustrated in Fig. 1(b). Source degeneration is used to increase the linearity of the aforementioned differential pairs.

For a given input, all except one of the differential pairs are saturated. The one differential pair that is active produces the shape of the fold around the reference voltage connected to one of its inputs. The zero-crossing points are controlled by reference voltages, therefore, the offset of each differential pair affects the linearity of the ADC directly. Offsets of differential pairs can be predicted by Pelgrom's law [10]. Transistor sizes must be large enough to ensure that the offset voltage is much smaller than one LSB of the ADC.

In order to generate fully differential folding current signals, the voltage difference ΔV_{ref} between two adjacent reference voltages in a folding block should satisfy

$$\Delta V_{\text{ref}} = |V_{\text{ref}}(i+1) - V_{\text{ref}}(i)| > 2 \cdot \sqrt{\frac{2I_{\text{BN}}}{\beta}}. \quad (2)$$

The above expression means that the linear regions of two adjacent differential pairs should not overlap each other.

C. Simple Current-Mode Interpolation Circuit

The current gain of a current mirror is controlled by the size ratio of the transistors. Therefore, we use a current-mode interpolator based on current mirrors. Current mirrors have wide bandwidth, thus, they are suitable building blocks for high-speed circuits. The accuracy of such an interpolator is limited by the mismatch of the transistors. The design parameter

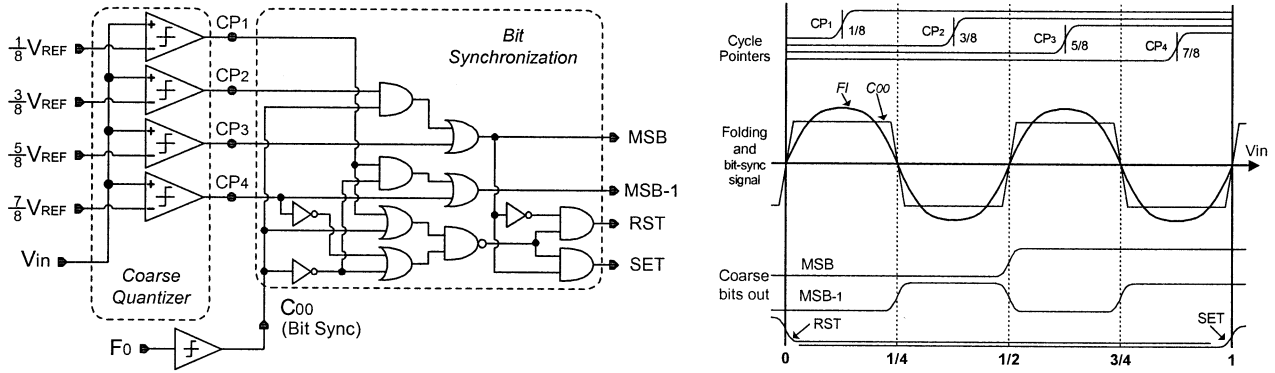


Fig. 6. Coarse quantizer and bit synchronization block diagram and waveforms. (Bit-sync signal C_{00} comes from fine quantizer and is the compared result from folding signal F_0 .)

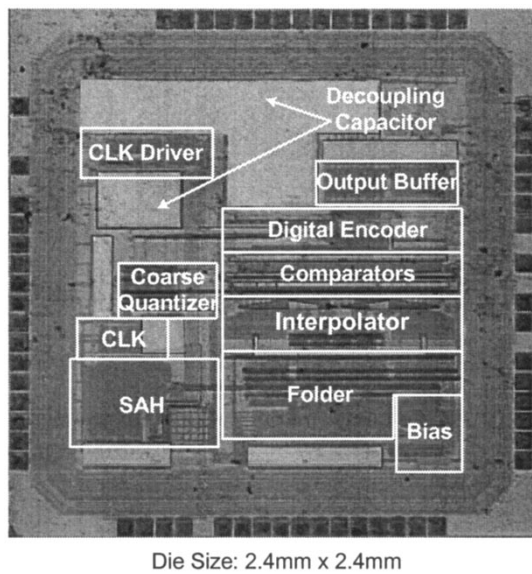


Fig. 7. F&I ADC die photo.

is the interpolation gain, which is determined by the size ratio between transistors MN2(MN4) and MN1(MN3) in Fig. 4. From an accuracy point of view, the impact of the following current comparators' offsets can be ignored if the combination gain of the folder and the interpolator is high enough. However, note that current mirrors with high current gain have lower bandwidth.

D. High-Speed Current Comparator

Comparators are used to detect zero-crossing points of all the folding currents from the interpolators. Because simple current mirrors are used in the interpolation block, voltage swings must be kept small to minimize errors caused by short channel effects. The current comparator we propose comprises a very low input impedance current-to-voltage interface and a normal voltage comparator, which consists of a preamplifier and a clocked latch. Transistors MN5 and MN6 in Fig. 4 form a feedback loop to reduce the input impedance. The small-signal input impedance of this transimpedance amplifier is

$$R_{in} = \frac{1}{g_{m6}} \cdot \frac{g_{o5}}{g_{m5}}. \quad (3)$$

TABLE I
ADC EXPERIMENTAL PERFORMANCE SUMMARY

Technology	2-poly, 4-metal, .35 μ m CMOS	
Supply Voltage	3.3V	
Input Range	1.6V p-p	
Active Area	1.2mm ²	
Resolution	7-bit	
Latency	2 Clock Cycles	
Conversion Rate	300MSamples/s	
Power Dissipation	200mW (@300MHz, excluding S&H)	
Differential Non-linearity	<0.6LSB	
Integral Non-linearity	<1.0LSB	
SNDR	38dB	33dB
Fin for SNDR measurement	60MHz	160MHz
SFDR	45dB	38dB
ADC input capacitance	2pF	
Chip Package	TQFP64	

In our design, the input impedance is small enough (about 50 Ω) to make the voltage swing at current-mirror outputs negligible. In comparison with the current comparators used in [6] and [9], our comparator has lower input impedance.

E. Bit Synchronization

Bit synchronization circuitry must be used in F&I ADCs because coarse and fine bits are generated independently. The schematic of the coarse quantizer and bit synchronizer is presented in Fig. 6. The coarse quantizer uses four voltage comparators to generate four cycle pointers CP_1 – CP_4 . Together with a bit-sync signal C_{00} coming from the fine quantizer, these four cycle pointers are used to generate the MSB and MSB-1. Waveforms are shown on the right-hand side of Fig. 6. In general, cycle pointers CP_1 and CP_4 are used for overflow and underflow detection. CP_2 and CP_3 are used to define the MSB. SET and RST are signals that indicate whether the input signal falls into the ADC input range. This information can be used to adjust the gain of the signal conditioning circuit preceding the ADC.

Note that the MSB and MSB-1 bits are not derived directly from the coarse quantizer; instead, they are determined by the bit-sync signal C_{00} , which comes from the fine quantizer (Fig. 1); thus, the offsets of the coarse quantizer comparators are not critical.

TABLE II
COMPARISON OF HIGH-SPEED LOW-RESOLUTION CMOS FOLDING AND/OR INTERPOLATING ADCs

Process	Bits	CLK (MHz)	SAH	Input BW (MHz)	Power (mW)	Area (mm ²)	Figure of Merit	Publication
0.5um BiCMOS	6	400	No	80	200@3.2V	0.6	25.6	JSSC1998 [2]
0.8um CMOS	8	70	No	6	110@3.3V	0.7	14	JSSC1995 [5]
1um CMOS	8	125	Yes	5	225@5V	4	6	JSSC1996 [3]
0.35um CMOS	8	200	No	10	210@3.0V	0.96	12.2	ISCAS2001 [6]
0.5um CMOS	8	100	Yes	4	165@5V	1.68	6.3	JSSC2001 [4]
0.5um CMOS	8	80	Yes	5	80@3.3V	0.3	16	ISSCC1996 [7]
0.18um CMOS	8	30	Yes	4	18@1.8V	0.96	57	VLSI2001 [8]
0.35um CMOS	6	50	No	2	20@1V	4.8	6.4	JSSC2000 [9]
0.35um CMOS	7	300	Yes	60	200@3.3V	1.2	38.4	This Work

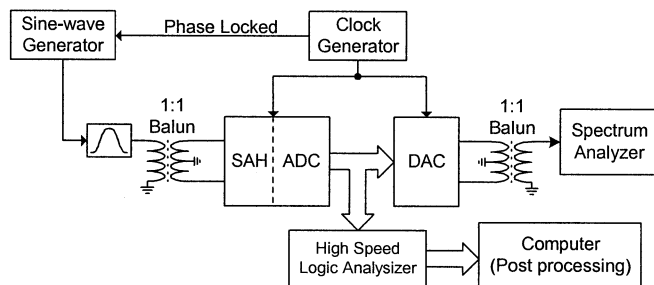


Fig. 8. Test setup.

IV. EXPERIMENTAL RESULTS

The ADC was fabricated in a four-level metal double-poly 0.35- μm CMOS process; only one poly layer was used, and the minimum gate length was 0.4 μm , using standard MOS field-effect transistors. We use only the components available in a digital process technology. The active chip area of the F&I ADC is 1.2 mm². A photomicrograph of the chip is shown in Fig. 7. Measured performance is summarized in Table I. At 300 MSamples/s, the ADC dissipates 200 mW from a 3.3-V power supply. A block diagram of the test setup is given in Fig. 8. Two high-speed synthesizers running with a common reference were used to generate clock and input signals.

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in Fig. 9. INL and DNL were generated using a code density (histogram) test [13] with a low-frequency sinusoidal signal. The spurious-free dynamic range (SFDR) and signal-to-noise-plus-distortion ratio (SNDR) are measured by postprocessing the acquired data with a discrete Fourier transform (DFT). Fig. 10 shows the SFDR versus analog input frequency at 300-MSamples/s operation. The effective number of bits drops to six when the input signal frequency is around 60 MHz.

The measured bandwidth of the F&I ADC is lower than Nyquist, the bandwidth is limited by the time-interleaving S/H. Although simulations show that S/H distortions are below -57 dBc when it acquires full-swing 160-MHz sine wave at 300 MSamples/s, the actual performance heavily depends on the matching between the two time-interleaving paths, which also relies on the placement and layout of components. The performance degradation due to timing mismatch becomes more serious at higher input frequencies, thus this time-interleaving

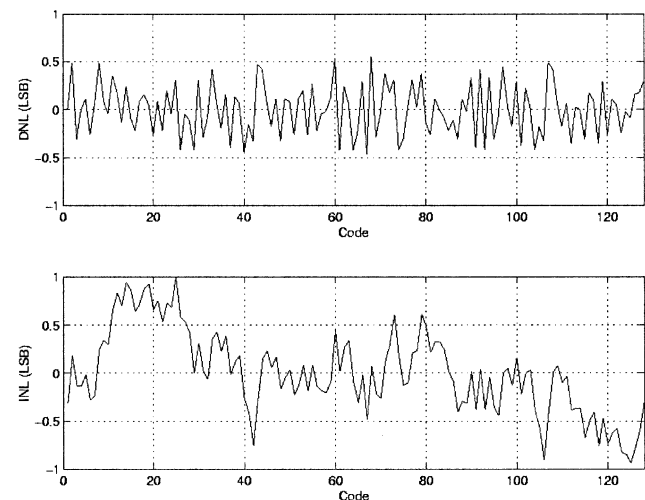


Fig. 9. Measured DNL and INL.

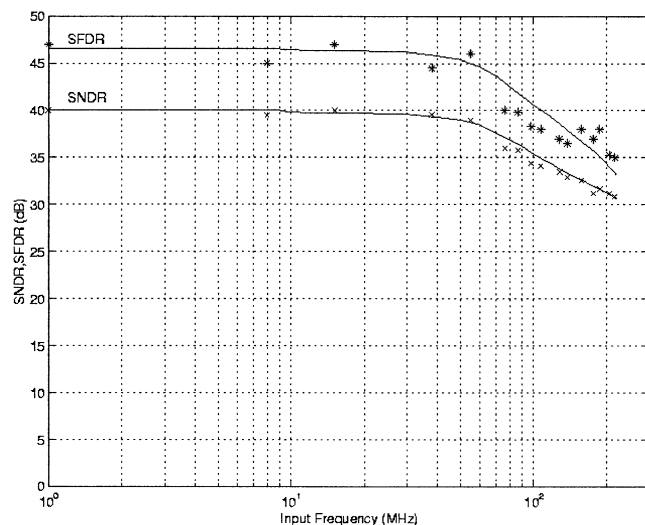


Fig. 10. Measured SNDR and SFDR versus input signal frequency.

architecture is not a good candidate for very high-frequency S/H unless self-calibration is employed.

Table II lists performances of some F&I ADCs appeared in the literature and this work, where the figure of merit is defined as $\text{FM} = ((2^n \cdot \text{BW}) / (\text{Power})) (\text{MHz/mW})$, where input resolution bandwidth BW is defined as the input signal frequency

at which the effective number of bits drops by 0.5 bit below dc resolution. In comparison with reported results, the proposed ADC achieves a resolution bandwidth of 60 MHz. The proposed F&I ADC yields a wide input bandwidth with relatively low power consumption and only requires conventional digital CMOS process technology.

V. CONCLUSION

Due to their unique folding analog preprocessing, F&I ADCs inherently have more serious bandwidth limitation problems than their full-flash counterparts. The positive impact of a front-end S/H on the frequency multiplication effect is substantial. Implemented in current mode, the folders and interpolators can reach higher bandwidth, and be compatible with lower power supply voltages. A very low input impedance current comparator is proposed to compare high-speed interpolated currents. A bit-synchronization scheme is proposed to not only correct errors caused by the delay difference between the coarse and fine quantizer paths, but also to detect the overflow and underflow. The result is a high-speed low-power F&I ADC with a wide input bandwidth.

REFERENCES

- [1] T. Yamamoto, S. Gotoh, T. Takahashi, K. Irie, K. Oshima, and N. Mimura, "A mixed-signal 0.18- μm CMOS SoC for DVD systems with 432-MS/s PRML read channel and 16-Mb embedded DRAM," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1785–1794, Nov. 2001.
- [2] M. Flynn and B. Sheahan, "A 400-Msample/s, 6-b CMOS folding and interpolating ADC," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1932–1938, Dec. 1998.
- [3] M. Flynn and D. Allstot, "CMOS folding ADCs with current-mode interpolation," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1248–1257, Sept. 1996.
- [4] M. Choe, B. Song, and K. Bacrania, "An 8-b 100-Msample/s CMOS pipelined folding ADC," *IEEE J. Solid-State Circuits*, vol. 36, pp. 184–194, Feb. 2001.
- [5] B. Nauta and A. Venes, "A 70-Ms/s 110-mW 8-bit CMOS folding and interpolating A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1302–1308, Dec. 1995.
- [6] S. Kim and M. Song, "An 8-b 200 MSPS CMOS A/D converter for analog interface module of TFT-LCD driver," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2001, pp. 528–531.
- [7] A. Venes and R. J. Plassche, "An 80-MHz 80-mW 8-b CMOS folding A/D converter with distributed T/H preprocessing," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 318–319, Feb. 1996.
- [8] T. Sigenobu *et al.*, "A 8-b 30-MS/s 18-mW ADC with 1.8-V single power supply," in *Proc. Symp. VLSI Circuits*, 2001, pp. 209–210.
- [9] B. Song, P. Rakers, and S. Gillig, "A 1-V 6-b 50-Msamples/s current-interpolating CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, pp. 647–651, Apr. 2000.
- [10] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1440, Oct. 1989.
- [11] K. Nagaraj, D. Martin, M. Wolfe, R. Chattopadhyay, S. Pavan, J. Cancio, and T. R. Viswanathan, "A dual-mode 700-Msamples/s 6-bit 200-Msamples/s 7-bit A/D converter in a 0.25- μm digital CMOS process," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1760–1768, Dec. 2000.
- [12] M. Choi and A. Abidi, "A 6-b 1.3-Gsample/s A/D converter in 0.35- μm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1847–1858, Dec. 2001.
- [13] J. Doernberg, H. Lee, and D. Hodges, "Full-speed testing of A/D converters," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 820–827, Dec. 1984.