

# A 3.3-V CMOS Adaptive Analog Video Line Driver With Low Distortion Performance

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**Abstract**—An analog line driver for video applications is presented. Utilizing a class-AB error amplifier structure, the design achieved 1.2-V peak-to-peak output swing with better than 42-dB linearity for frequencies up to 5 MHz. An adaptive tuning scheme for output impedance matching using peak detection is used to provide uniform performance across line impedance variations. The circuit is designed in AMI 0.5- $\mu$  CMOS technology and has a tuning range of 70–180  $\Omega$  with a power consumption of about 26.4 mW at 75- $\Omega$  load.

**Index Terms**—Adaptive circuits, class AB, CMOS, line driver.

## I. INTRODUCTION

THE demand for information has led to the development of several low-cost high-data-rate systems. The important link between the sophisticated digital signal processing (DSP) algorithms and the analog signals riding the cable are hybrid circuits, of which the line driver is a key element. Line drivers find application in ISDN transceivers, DSL, and cable modems to drive the analog signals onto the communication channel or medium. The line driver is part of the analog front-end transmitter for a wired communication system and is analogous to the power amplifiers in wireless transmission. Line drivers are voltage buffers that provide the necessary output current to drive the small load impedance (nominally matched to the line impedance), which is nominally between 50 and 150  $\Omega$  and varies upon the cable length, temperature, and other external effects. The main requirements of a line driver are high output swing, high linearity, good power efficiency, and matching for line impedance over process variations.

The attenuation along the cable is exponentially proportional to the cable length and radius. As a result, high output swing is required so that the signal can be differentiated from the noise at the receiver end or at a repeater. Furthermore, modulation techniques such as discrete multitone (DMT) distribute information in discrete tones that can be treated as pseudorandom noise in time domain [1]. These tones add up to create high crest factor (peak-to-average voltage ratio), which can exceed the linear range of the amplifier, causing signals to be distorted.

One of the important parameters of a communication system is the bit-error rate (BER) at the receiver, which is correlated with the distortion in the analog transceiver blocks [1]. High dynamic range of the line driver ensures lower BER of the overall system. Also due to the large output swing and small load (line) impedance, high power efficiency is demanded.

Usually, class-AB output stages provide best results in terms of efficiency and swing. The line impedance is subject to large variations due to loading effects, line length variation, and temperature [2]. Without matching, the reflections are not canceled at the transmitter end, which may degrade the driver performance. Thus, tuning and matching of the output impedance of the driver to the load is necessary to achieve maximum power transfer while maintaining high linearity.

Several line driver architectures for different applications (Serial Bus, Video, xDSL, and ISDN) are extensively available in the literature, with emphasis on linearity, output swing, power efficiency, bandwidth, and matching. An ISDN line driver [3] has been designed with 80-dB linearity and 2.5-V<sub>P-P</sub> (peak-to-peak) swing by trading off output swing of the buffer to the transformer ratio. An HDSL line driver with resistive feedback and Miller compensation [4] achieved 70-dB linearity and 2.4-V<sub>P-P</sub> swing with 30- $\Omega$  load resistance. Using a fully differential architecture with gain tuning [5] achieves better than 47-dB linearity with a 75- $\Omega$  load. The reported power efficiency is, however, poor. In [5]–[7] tuning schemes are utilized for gain, impedance, or quiescent current adjustment to achieve similar results over a range of operating conditions.

This paper describes a CMOS line driver capable of delivering 1.2-V<sub>P-P</sub> signal up to 5 MHz with a linearity (SFDR) of better than 0.4% across load variations from 70 to 180  $\Omega$ . The emphasis of the design is on impedance matching, thereby maximizing power efficiency. Using an on-chip tuning scheme with continuous calibration, the output impedance of the line driver is matched to the line impedance, providing uniform line driver performance across a range of line impedance variation.

Section II outlines the principle behind impedance matching and the need for proper termination in line driver circuits. In Section III, the proposed video line driver with the associated tuning circuitry is presented. Section IV provides the experimental results from the chip, and conclusions are drawn in Section V.

## II. BASIC PRINCIPLE

While transmitting high-speed data over communication channels, proper matching of impedance at both the driver and the receiver end is necessary to ensure low BER. When a signal encounters a mismatch in impedance due to improper termination, reflections or echoes appear on the line, whose characteristics depend on the line length and signal frequency [9]. Such reflections distort the information and reduce the bit rate of the system.

A simple solution commonly used to eliminate reflections at the driver end is to use series termination as shown in Fig. 1,

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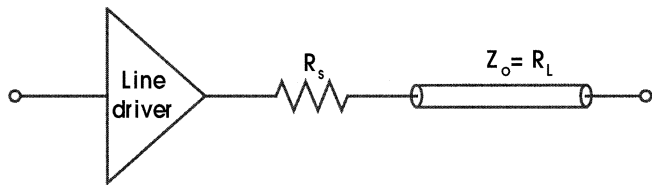


Fig. 1. Series termination at line driver end.

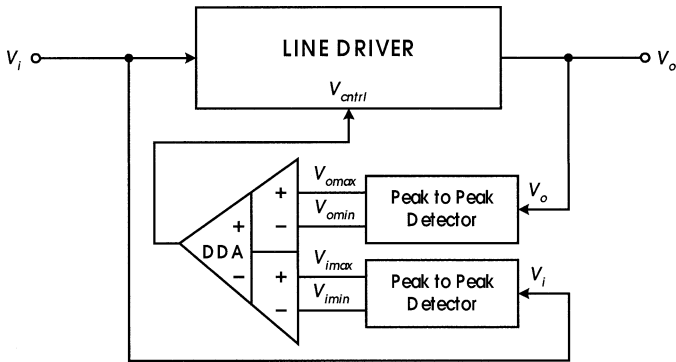


Fig. 2. System block diagram with the line driver and tuning loop.

where  $Z_o$  denotes the line impedance of the cable. The resistance  $R_S$  is chosen such that the sum of the output resistance of the line driver and series resistor ( $R_S$ ) equals the nominal line impedance ( $Z_o$ ). However, this scheme has several inherent disadvantages. Process variations cause the output resistance of the line driver to vary, requiring the termination resistor to be changed accordingly. In addition to this, the line impedance is also subject to variations. A second serious drawback is the voltage drop across the resistor. If the output resistance is neglected,  $R_S$  is equal to  $Z_o (=R_L)$ , in which case half the voltage is lost across  $R_S$ . Consequently, the signal swing requirement is now doubled as compared to the unterminated case, with the linearity and power-supply conditions unchanged.

To overcome these drawbacks, the design approach is to match the output impedance of the buffer directly to the line impedance, thereby eliminating the need for series termination and avoiding the associated voltage drop. Impedance matching is done using a topology wherein, when the output voltage is equal to the input, the output resistance is matched to the line. This scheme has the advantage that it can adjust to external line as well as internal process variations.

The origin of the architecture presented in this paper is the class-A adaptive line driver [7], [8] with a tuning scheme which utilizes dc operating point correction for impedance matching. This topology, however, is limited in its power efficiency due to the class-A operation. In order to provide 1.2- $V_{P-P}$  swing, a dc current of at least 8–10 mA is required to provide the necessary dc operating point at the output. By extending the topology to a push-pull class-AB structure, the efficiency can be improved significantly. A robust tuning scheme employing peak detection is combined with the line driver to provide consistent performance across varying line impedance.

Fig. 2 shows the overall block diagram of the proposed video line driver with the tuning loop consisting of the peak-to-peak detectors and a differential difference amplifier. Using the peak-to-peak detectors, positive and negative peak voltages

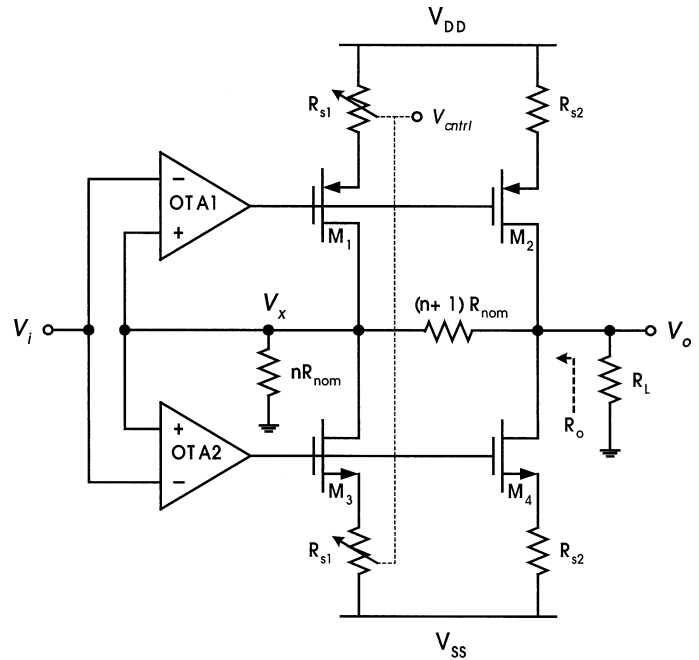


Fig. 3. Line driver schematic with the error amplifiers, class-AB output stage, and tunable current mirrors.

of the input and the output are extracted. With the differential difference amplifier (DDA) and the four outputs of the peak detector block, the control voltage  $V_{ctrl}$  is obtained, completing the feedback loop. This control voltage is used to adjust the mirroring factor of the tunable current mirrors in the line driver. When the line impedance increases, the current delivered is decreased and vice versa, such that the same output voltage as the input is obtained. When the input and output voltages are forced to be equal, the output resistance of the driver is matched to that of the line.

### III. LINE DRIVER DESIGN

Although designed for specific line impedance, line drivers need to adapt themselves to variations in line characteristic impedance; otherwise, the linearity and the output swing of the line driver will be adversely affected. In this paper, a class-AB output stage with controlled output impedance is used as a line driver architecture wherein the mirroring factor is adjustable. The mirroring factor is adjusted through the feedback loop and controls the gain and output resistance of the driver.

#### A. Class-AB Output Stage

The line driver schematic as shown in Fig. 3 consists of a class-AB output stage with error amplifiers whose output resistance is controllable. Although the quiescent current control is an important design constraint [10], [11], the line driver proposed in this paper lacks a quiescent current stabilizer circuit since the main motivation in this design is to apply impedance tuning to a class-AB buffer. The quiescent current is set by the gate-to-source voltages of  $M_2$  and  $M_4$ , which is further controlled by the error amplifiers in feedback. The error amplifiers are designed with low gain so that offsets or mismatch do not cause large variations in the quiescent current.

In Fig. 3, the dc voltage at the nodes  $V_x$  and  $V_o$  are identical to the input, assuming zero offset voltages for the error amplifiers. Any mismatch between the mirroring ratios of the half-circuits and the input offsets of the error amplifiers cause small dc currents to flow across the bridge resistance. Error amplifiers are designed with sufficient gain to ensure that the signal  $V_i$  is copied to the node  $V_x$ . The signal current ( $V_x/nR_{\text{nom}}$ ) is mirrored by the transistors  $M_1$ – $M_2$  and  $M_3$ – $M_4$  to the output stage, summed at the node  $V_o$  and flows into  $R_L$ . The dc operating point and the large signal operation of the line driver is unaffected by the bridge resistance, which sees only the signal reflections from the line. The overall buffer gain and the output resistance  $R_o$  are given in (1) and (2), respectively. Under the assumption that transistors  $M_1$ – $M_4$  are in saturation, the following expressions are valid

$$\frac{V_o}{V_i} = \frac{m}{n} \frac{R_L}{R_{\text{nom}}} \quad (1)$$

$$R_o = \frac{n+1}{m+1} R_{\text{nom}} \quad (2)$$

$$n = \frac{W_2/L_2}{W_1/L_1} = \frac{W_4/L_4}{W_3/L_3} \quad (3)$$

$$m = \frac{I_{D2}}{I_{D1}} = \frac{I_{D4}}{I_{D3}} = n \frac{(V_{GS2} - V_{Tp})^2}{(V_{GS1} - V_{Tp})^2} = n \frac{(V_{GS4} - V_{Tp})^2}{(V_{GS3} - V_{Tp})^2}. \quad (4)$$

The ratio  $m$  defines the mirroring factor of transistor pairs  $M_1$ – $M_2$  and  $M_3$ – $M_4$  and is a function of both the transistor dimensions and gate-to-source voltages ( $V_{GS}$ ), while  $n$  is a ratio of device dimensions. Thus the value of  $m$  equal to  $n$  is a special case, when the line resistance is  $R_{\text{nom}}$ . Furthermore, the variable resistor  $R_{S1}$  controls the source voltage ( $V_S$ ) of transistors  $M_1$  and  $M_3$ . The tuning loop enforces the output voltage to be equal to the input, which results in the condition given by

$$\frac{m}{n} \frac{R_L}{R_{\text{nom}}} = 1 \Rightarrow R_{\text{nom}} = \frac{m}{n} R_L \quad (5)$$

where  $R_{\text{nom}}$  and  $n$  are fixed by design to be  $75 \Omega$  and 12, respectively. When  $R_L$  increases, the mirroring ratio  $m$  decreases to satisfy the condition in (5). Substituting (5) in (2) results in the output resistance being equal to the line resistance as in

$$R_o = \frac{n+1}{m+1} R_{\text{nom}} = \frac{n+1}{m+1} \frac{m}{n} R_L \approx R_L. \quad (6)$$

Thus, using this line driver architecture, when the output is made equal to the input, the output resistance of the driver is equal to that of the line and a proper line termination is achieved. The mirroring ratio  $m$  is mainly determined by the variable resistance  $R_{S1}$  which is controlled through the feedback loop. If the gate-to-source voltage  $V_{GS}$  of the transistors  $M_1$ – $M_2$  and  $M_3$ – $M_4$  are the same, the mirroring ratio  $m$  is determined by the transistor aspect ratios ( $M_1$ – $M_2$  and  $M_3$ – $M_4$ ) and is equal to  $n$ . This occurs when the load resistance  $R_L$  is the same as  $R_{\text{nom}}$ . When the load resistance  $R_L$  decreases, the signal current is increased in order to maintain the same output swing as the input. This is achieved by increasing the resistance  $R_{S1}$ , which consequently increases  $V_{G3}$  and decreases  $V_{G1}$ . However, the gate-to-source voltages of  $M_1$  and  $M_3$  do not change. This is because the source voltage  $V_S$  tracks the gate voltage  $V_G$ . On

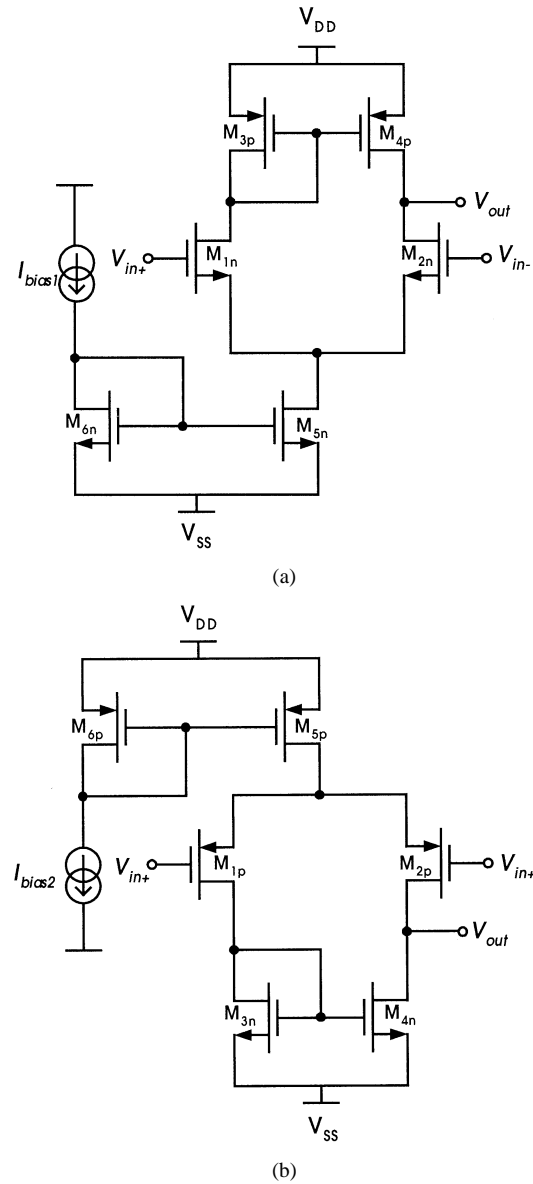


Fig. 4. (a) Positive-half (OTA1) and (b) negative-half (OTA2) error amplifiers.

the other hand,  $|V_{GS2}|$  and  $|V_{GS4}|$  increase, which results in an increase in the mirroring ratio  $m$  as seen from (4).

### B. Transconductors

Positive-half (OTA1) and negative-half (OTA2) error amplifiers (Fig. 4) are basic differential amplifiers with n- and p-type drivers, respectively. Using such complementary structure is crucial to handle large signal swings for both the negative and positive cycle. The differential amplifier with nMOS drivers can handle input common mode signals as high as  $(V_{DD} - V_{GS, M3p} + V_{T, M1n})$  which makes it a good positive-half error amplifier. On the other hand, the amplifier with pMOS drivers can handle input common-mode signals as low as  $(V_{SS} - V_{GS, M3n} + V_{T, M1p})$ , which makes it appropriate as a negative-half error amplifier.

The dc gain of the error amplifiers is around 30–35 dB. Low gain causes error in signal voltage when copied from  $V_i$  to  $V_x$  and then to the output  $V_o$ . On the other hand, high gain causes

large variations in gate-to-source voltages in the presence of offset and mismatch [12]. This results in a large increase in the quiescent current and distortion. The gain-bandwidth product of the transconductors is greater than 300 MHz, which ensures negligible phase shift from input to output, in the frequency band of interest (10 kHz to 5 MHz). This condition ensures a robust tuning scheme through the comparison of the input and output envelopes, even with a simple peak detector. An important concern is the combined input offsets of the error amplifiers when used in closed loop. This affects the dc node voltage at  $V_1$  and  $V_o$  and can cause considerable output offset and quiescent current variations.

### C. Linearized Variable Resistor

In the line driver of Fig. 3, the signal current in the intermediate stage ( $M_1$ – $M_3$ ) is fixed at  $V_x/nR_{nom}$ . Thus, the mirroring ratio  $m$  is adjusted by the tuning loop to deliver the appropriate current to the output ( $M_2$ – $M_4$ ) stage in a way that will maintain the unity gain of the buffer across varying line conditions. Resistor  $R_{S1}$ , implemented as a poly-resistor in parallel with an nMOS/pMOS device as shown in Fig. 5(a) and (b). The resistance value can be adjusted through  $I_{tune}$ , which is generated from the control voltage  $V_{ctrl}$  as shown in Fig. 5(c). The gate voltage of the MOS transistors ( $M_{Pres}/M_{Nres}$ ) controls the effective resistance  $R_{S1}$ . This current is mirrored to the output and flows through  $R_L$ . In order to eliminate the nonlinearity of the resistor, the source of the transistors are biased with  $V_{DS}/2$

$$I_D = K \left( (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (7)$$

$$V_{GS} = V_{GSO} + \frac{V_{DS}}{2} \Rightarrow I_D = K(V_{GSO} - V_T)V_{DS}. \quad (8)$$

Since the transistors operate in the triode region, ignoring higher order effects, this biasing scheme reduces the nonlinearity of the resistor.  $I_D$  and  $V_{GS}$  in (7) and (8) are the drain current and gate–source voltage of  $M_{Pres}$  and  $M_{Nres}$ , respectively.

### D. Peak-to-Peak Detector and DDA

In order to generate the control voltage  $V_{ctrl}$ , a peak-to-peak detector circuit, as in Fig. 6, in combination with a DDA shown in Fig. 7 is utilized. The detector circuit consists of two circuits, one each for the positive and negative peak values. The first stage acts as a peak detector, wherein the capacitances  $C_2$  and  $C_3$  are charged to the positive and negative peaks quickly and discharged at a very slow rate by a small current. The second stage reduces the dc shift from the first stage so that the dc point at the output is close to the input and applies a second peak detection to the output of the first stage, further reducing the ripple. The transient response of the peak-to-peak detector for a  $1-V_{p-p}$  input signal at 2 MHz is shown in Fig. 8(a) with the positive and negative peak signals. The ripple in the peak values is about 30 mV. By using smaller discharge currents, the ripple can be reduced.

Two identical peak-to-peak detectors are used for the inputs and the outputs. Systematic mismatch between the positive or negative peak detector circuits for the inputs and outputs is not of much concern since they are cancelled at the inputs of the

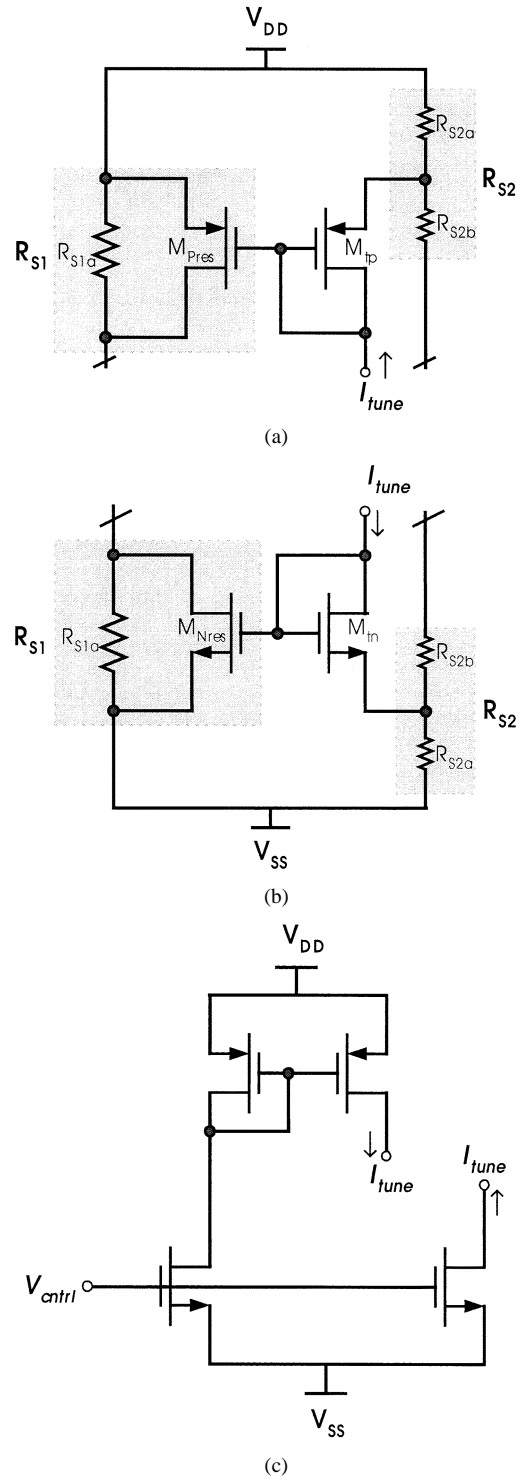


Fig. 5. Tunable resistor implementation. (a) P-type variable resistor with linearization. (b) N-type variable resistor with linearization. (c) Resistor control through  $I_{tune}$ .

differential difference amplifier. However, random mismatches including wafer gradients can offset the tuning process, causing poorer matching. The positive and negative peak values of the input  $V_i$  are available at  $V_{i,max}$  and  $V_{i,min}$ , which are not significantly dependent on the dc offset as shown in Fig. 8(b). Two such peak detector circuits are used to obtain the four peak voltages of the line driver input and output ( $V_{i,max}$ ,  $V_{i,min}$ ,  $V_{o,max}$ , and  $V_{o,min}$ ).

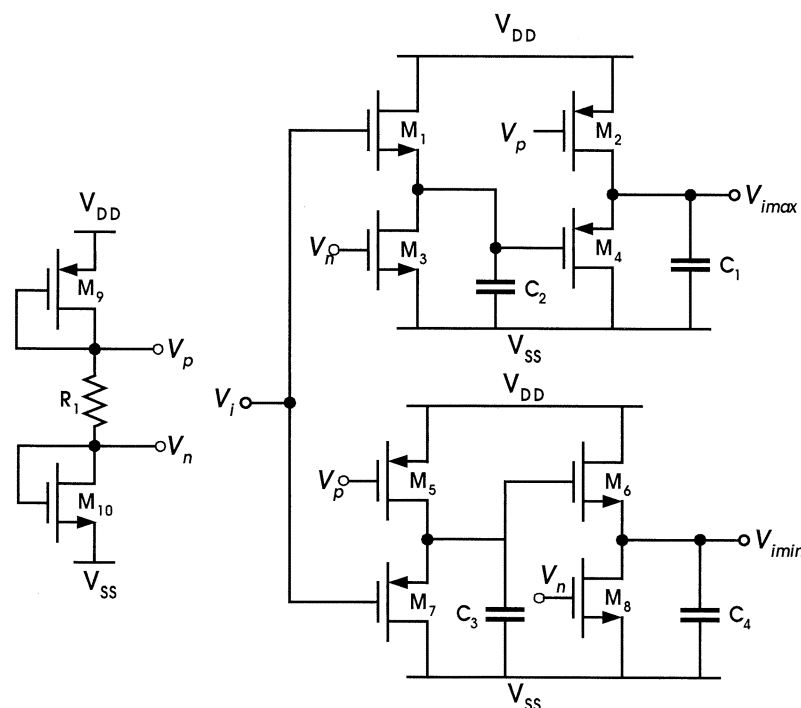


Fig. 6. Peak-to-peak detector.

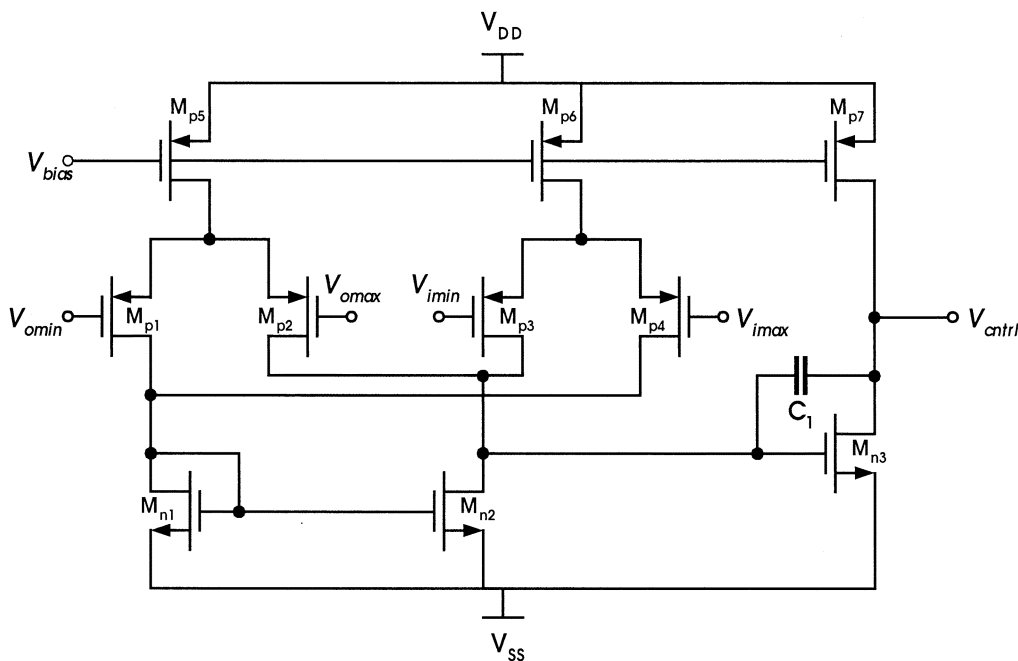


Fig. 7. Differential difference amplifier.

When a sinusoid is applied to the line driver input, the instantaneous output voltage may be different from the input depending on the line conditions. The peak-to-peak information of the input and output are detected and the control voltage ( $V_{ctrl}$ ) is computed by the DDA. The tuning current ( $I_{tune}$ ) further generated from the control voltage adjusts the variable resistor  $R_{s1}$  suitably to increase or decrease the mirroring ratio, thereby completing the tuning loop. When the output voltage is less than the input, the mirroring ratio is increased and vice versa. Thus, for a

range of line impedance variations, the line driver gain is unity and the output impedance matched to that of the line.

#### IV. EXPERIMENTAL RESULTS

The circuit of Fig. 3 along with the tuning loop is integrated in a standard 0.5- $\mu\text{m}$  CMOS process. The active area is about 0.22  $\text{mm}^2$ . The input signal for tuning purposes is a 1- $V_{p-p}$  sinusoid at 5 MHz. The choice of the test signal is determined by the

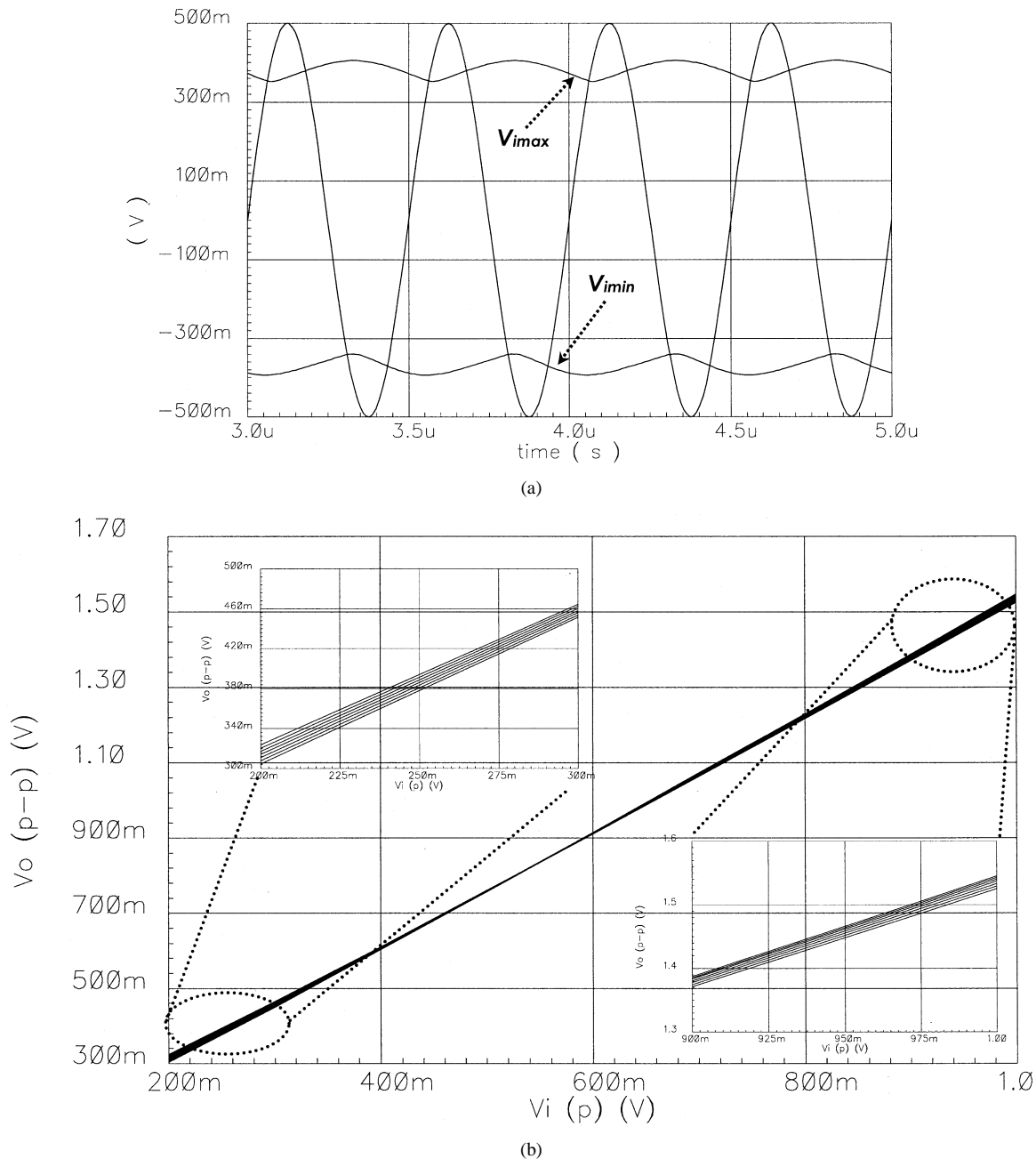


Fig. 8. (a) Transient response of the peak-to-peak detector. (b) Output peak-to-peak voltage versus input peak voltage for different input offsets.

tuning loop. The input amplitude is chosen as high as possible, without saturating the line driver (typically  $1\text{--}1.4 V_{P-P}$ ). This is because the peak detector does not give the exact peak value and has a limited input range between  $0.4$  and  $1.2 V_{P-P}$ . As a result, for small input voltages (around  $200$  mV), the tuning loop does not converge properly. The frequency of the signal should be close to the maximum operating frequency of line driver so as to filter out the signal components and obtain a steady-state control voltage  $V_{CTRL}$ . Simulation results indicate the overall settling time response of the tuning loop to be about  $50 \mu\text{s}$ .

The line driver gain response with and without impedance matching is shown in Fig. 9. In the absence of tuning, the output voltage exceeds or is less than the input. The signal current supplied to the load is a fixed multiple  $m$  of the current generated by  $M_1$  and  $M_3$  (determined by resistance  $nR_{nom}$ ), irrespective of

the line impedance. However, in the case of tuning, variable current is provided to the load by adjusting the mirroring ratio  $m$ , thereby forcing the output to follow the input. Thus, as load resistance increases, current is decreased to achieve constant output. The tuning range in this case varies from  $70$  to  $180 \Omega$  for less than 3% error between input and output voltage.

While impedance matching to provide uniform performance is essential, the linearity of the line driver cannot be sacrificed. This imposes additional constraints to the design in terms of distortion specifications. Fig. 10 shows the distortion performance for  $75\text{-}\Omega$  line impedance and  $1\text{-}V_{P-P}$  output at  $2$  MHz measured using an HP4395 spectrum analyzer. The second harmonic is lower than 45 dB compared with the input and improves with lower frequency. Fig. 11 shows the linearity measurement as a function of frequency for three different line resistances at

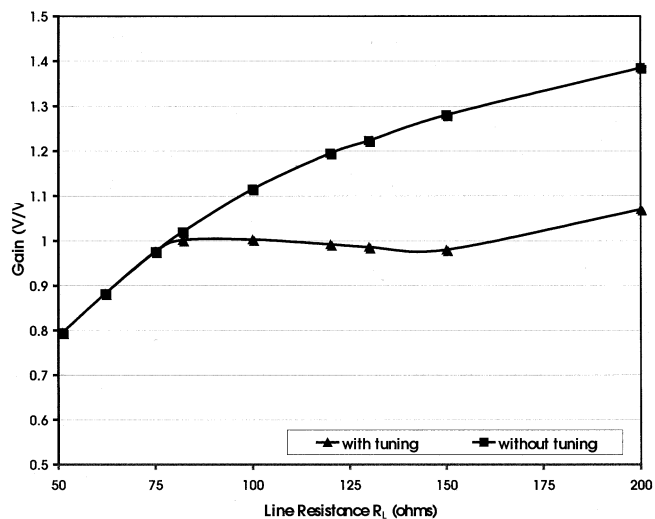


Fig. 9. Gain ( $V_o/V_i$ ) as function of line resistance  $R_L$  with and without tuning.

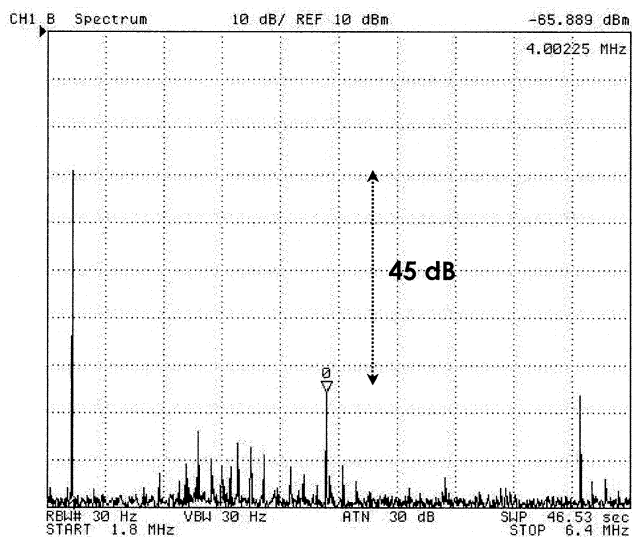


Fig. 10. Frequency spectrum at 75- $\Omega$  load, 1  $V_{p-p}$ , 2-MHz input.

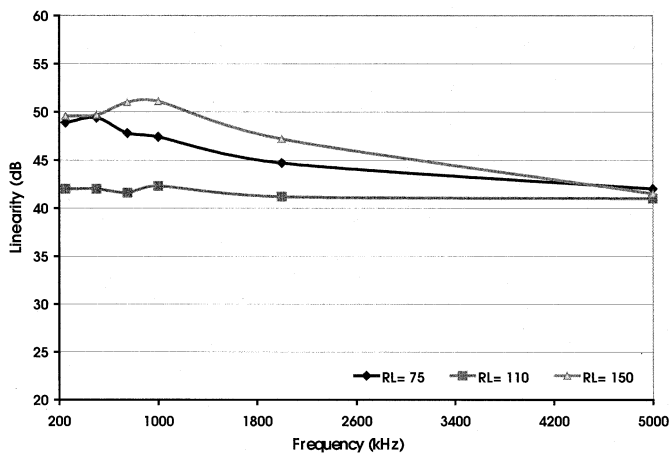


Fig. 11. Linearity as a function of frequency for different  $R_L$ .

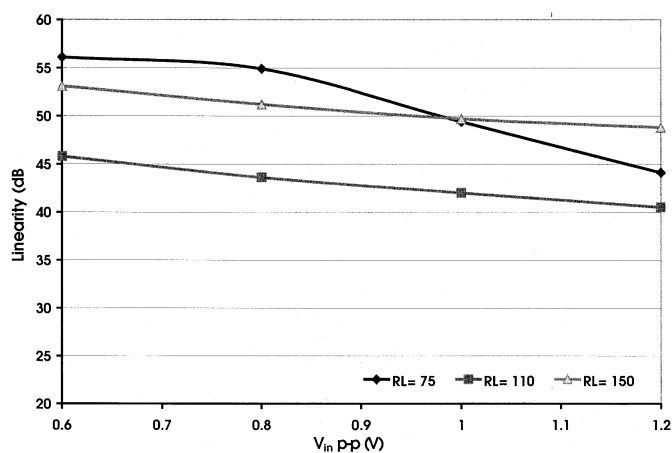
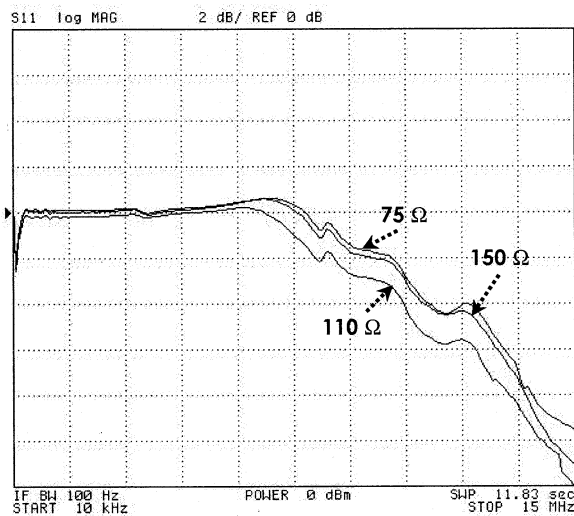
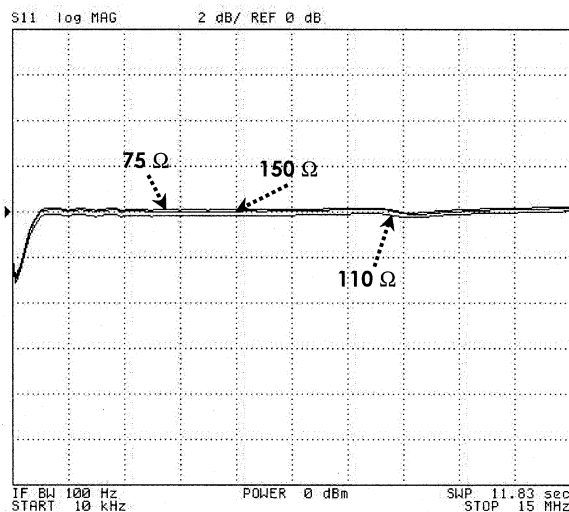


Fig. 12. Linearity as a function of input voltage for different  $R_L$ .



(a)



(b)

Fig. 13. AC response of the line driver for line resistance  $R_L$  of 75, 110, and 150  $\Omega$ . (a) 10 kHz to 15 MHz. (b) 10 kHz to 5 MHz.

1  $V_{p-p}$ , while Fig. 12 shows linearity against input voltage for 500-kHz input frequency. The overall line driver performance

is better than 42 dB over the frequency range from 10 kHz to 5 MHz, with 1.2- $V_{p-p}$  output.

TABLE I  
SUMMARY OF LINE DRIVER PERFORMANCE

Technology	0.5 $\mu$ m CMOS (3 AL, 2 PS)
-3 dB bandwidth	15 MHz (10 pF load)
Gain Flatness	0.1 % up to 5 MHz
Tuning range	70 to 180 $\Omega$
Linearity (SFDR) (10 kHz - 5 MHz)	> 42 dB (1.2 V <sub>p-p</sub> )
Slew Rate	31.3 V/ $\mu$ s
Voltage Supply	$\pm 1.5$ to $\pm 3$ V
Quiescent Power Consumption	26.4 mW @ $\pm 1.65$ V
Maximum Output Swing	1.6 V peak-to-peak
Maximum Power Efficiency (@ 75 $\Omega$ )	16.1 %
Active Area	.22 mm <sup>2</sup>

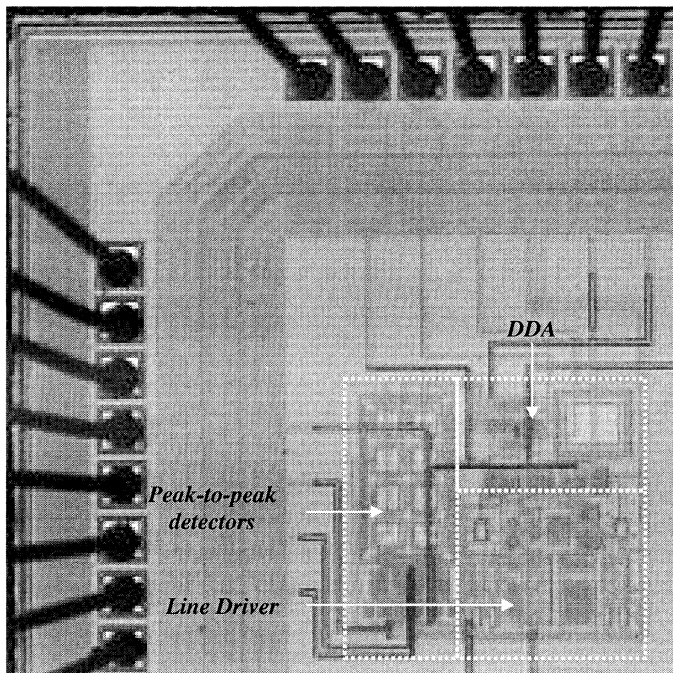


Fig. 14. Line driver chip microphotograph.

The gain versus frequency response was measured using an HP4395 network analyzer. The ac response is shown in Fig. 13(a) for the line driver at 75-, 110-, and 150- $\Omega$  line impedance. The bandwidth in all cases is around 15 MHz due to the loading of the output stage. The gain is one in the case of 75- and 150- $\Omega$  load, while it is 0.98 at 110  $\Omega$ , an error of 2%. The gain flatness is accurate to 0.1% variation up to 5 MHz as seen in Fig. 13(b).

Table I summarizes the experimental results of the line driver. Across a wide range of line impedance, the linearity (SFDR) has been shown to be consistently better than 42 dB for 1.2-V swing and gain response is unity with an error of less than 3%. The power consumption is 27 mW, 30% of which is consumed by the tuning loop. The line driver can be easily scaled for different supply voltages from 3 to 6 V. The input signal amplitude has to be correspondingly scaled to achieve best results. The chip is fabricated in AMI 0.5- $\mu$ m CMOS three-metal two-poly process. The die photo is shown in Fig. 14.

## V. CONCLUSION

A compact 3.3-V 0.5- $\mu$ m CMOS analog line driver is presented. The main features of this line driver are the class-AB output stage with the controlled output impedance and the tuning scheme as compared with the previous architecture [7]. This line driver topology provides proper line termination while eliminating the drawbacks associated with series line termination such as voltage drop across the matching resistor. The tuning scheme, simple yet robust, provides wide matching range from 70 to 180  $\Omega$ . A maximum power efficiency of 16% is achieved with an output voltage range of  $\pm 0.8$  V. Linearity can be improved by making the line driver pseudo- or fully differential and by implementing a quiescent current control loop.

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