also turn off and N3 will turn on, and node 2 will discharge to 
zero. Nodes 1 and 2 drive the slave-latch and the output Q will 
become low. The threshold voltage of the MOSFETs is 0.7V, but 
with a backgate bias $V_{gs}$ of 6V, the threshold voltage of P1 and 
P2 will become $-1.5V$, which is high enough to cut off the leakage 
current with a 2V clock swing for 3.3V $V_{cc}$.

The operation waveform of the proposed flip-flop is illustrated 
in Fig. 2, which is obtained by HSPICE simulation. In Fig. 3, we 
compare the voltage current $I(V_{dd})$ of the previously proposed 
flip-flop [2] and the flip-flop proposed in this Letter. The proposed 
flip-flop restrains the superfluous recharging and discharges so 
that the current of the supply power is obviously reduced.

In this proposed flip-flop, the power dissipation reduction 
depends on the input data pattern. The proposed flip-flop has a 
precharge and discharge scheme so that the worst condition occurs 
when the transition probability is 50%. The simulation results also 
show that when the input data’s transition probability is 50% the 
proposed flip-flop can lead to a saving of $\approx 50\%$ in power 
consumption compared to the reduced clock swing flip-flop proposed 
in [2]. When the input data’s transition probability is $> 50\%$, the 
conditional precharge scheme ensures that the precharge and dis- 
charge will not proceed whenever the input data remains fixed, so 
the power saving is increased over that for previous patterns.

Conclusion: We have proposed a small clock swing flip-flop based 
on a new precharge scheme. Using the new precharge scheme, the 
proposed flip-flop can lead to a reduction in the power consumption 
by at least 30% compared to previously proposed reduced clock 
swing flip-flops.

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True background calibration technique for 
 pipelined ADC

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A digital background calibration technique for a pipelined 
analogue-to-digital converter (ADC) is presented. The calibration 
technique involves the use of a superior, low-accuracy, ADC in 
conjunction with a least-mean squares (LMS) algorithm to find 
the parameters, which correct for residue errors such as finite op-
amp gain error, capacitor ratio mismatch and charge injection 
error in a non-ideal pipeline stage, resulting in a significant 
improvement in the INL and the DNL of the ADC.

Introduction: Pipelined analogue-to-digital converters (ADCs) 
have been widely used in high speed, high resolution applications. 
With the advent of broadband networks, the resolutions required 
from these converters is continually increasing. In a conventional 
switched-capacitor pipelined ADC the accuracy is fundamentally 
limited by capacitor mismatch and the finite amplifier gain. Self-

Fig. 3 $V(V_{dd})$ comparison of previous and proposed flip-flops

--- $V(V_{dd})$ of previous flip-flop proposed in [2]
--- $V(V_{dd})$ of proposed flip-flop

Calibration techniques have been proposed recently [2, 3]. One method of 
background calibration is to employ an extra pipeline stage that is 
used to substitute for the stage being calibrated [3]. The disadvan-
tage of this technique is that it results in fixed pattern noise due to 
the periodic substitution of stages. Another proposed background 
calibration scheme requires the addition of a calibration signal to 
the input. This results in a reduction of the useful dynamic range 
of the converter. In this Letter we describe a true background cal-

Fig. 1 N-stage 1 bit per stage pipelined ADC prototype

...
Proposed calibration scheme: The proposed background calibration algorithm is shown in Fig. 2. The basic idea here is to correct for the residue errors in a non-ideal pipeline stage by comparing its residue (Vresid) with an ideal estimate (Videal) generated using an accurate calibration stage that receives the same analogue input as the non-ideal stage under calibration. Vout is then processed using a function block F, which generates an estimate Vcalc of the ideal residue voltage. The aim of the correction algorithm is to find the correct parameters for the function block F so that Vcalc is as close to Vresid as possible. A gradient-descent (LMS) approach is used as a correction algorithm, to be discussed later. To correct for residue errors in a non-ideal pipeline stage, we just need the correct estimate of the slope and y-intercepts of the residue curve for V < Vout and V ≥ Vout, where Vout is the bit threshold decision of the comparator in a pipeline stage. Hence, the function F can be a linear function of its input of the form F(V) = αV + β, where V is the input voltage (non-ideal residue output) to the function block. We may have two sets of (α, β), one for V < Vout and the other for V > Vout, for each pipeline stage to be calibrated. These parameters would then be used during conversion to generate the calibrated digital output.

![Diagram showing proposed calibration algorithm](image)

Fig. 2 Basic idea of proposed calibration algorithm

The error e between the estimate and the ideal residue voltage for the same input is then given by Vcalc - Vresid. We start with an unknown value for the parameter set (α, β), and at every step, we compute the mean square error gradient and update the parameters in the direction of decreasing gradient. The update algorithm for the parameter set (α, β) can be given by

\[ \alpha_{new} = \alpha_{old} + \mu V_{out} \]
\[ \beta_{new} = \beta_{old} + \mu e \]

where \( \mu \) is the update step size for the gradient descent algorithm. The above algorithm converges to the desired parameter set (α, β) such that e = 0, Vcalc = Vresid. For ease of implementation and to remove multipliers, a modified sign implementation of the gradient descent algorithm can be used:

\[ \alpha_{new} = \alpha_{old} + \mu \text{sgn}(e) \text{sgn}(V_{out}) \]
\[ \beta_{new} = \beta_{old} + \mu \text{sgn}(e) \]

where \( \text{sgn}(e) = 0 \) if \( e = 0 \), otherwise \( \text{sgn}(e) = 1 \) if \( e \) is positive and \( \text{sgn}(e) = -1 \) if \( e \) is negative. On the other hand, \( \text{sgn}(e) \) returns the sign of the argument. As the parameters change slowly with time, we need to run the calibration only once in thousands of cycles. This relaxes the speed requirements in the design of an ideal calibration stage.

Complete implementation of calibration algorithm: Consider an 8 bit pipelined ADC for illustration. Assume that the first four stages need to be calibrated. Also, assume that stages 5-8 are ideal, for illustration purposes. Calibration begins with stage 4 which is the least significant stage to be calibrated. The slow but accurate pipeline stage in Fig. 2 is replaced by a slow, but accurate, ADC which itself can be a self-calibrated algorithmic ADC. This ADC provides a digital word representation of the ideal residue (Videal) for the stage under calibration (stage 4). Let Dideal represent such a digital word equivalent of the ideal residue. Since the residue voltage from stage 4 (Vresid) is sampled as the input by the following stages, the digital equivalent of the residue output of stage 4 can be given by the word D0D1D2D3. The gradient descent algorithm (eqn. 1) can now be used to estimate the parameters (α, β) of the function block F = f(V) for stage 4 using the above digital word equivalents for the residues. Once the parameters for stage 4 have been obtained, we calibrate the next most significant stage (stage 3). The slow but accurate ADC is now connected in parallel with stage 3.

The back-end of the pipeline consists of a calibrated non-ideal stage 4 and ideal stages 5-8. Therefore, the digital equivalent of the residue of stage 3, Vresid, is equal to the value 2D0 + D1D2D3. Dideal gives the digital word equivalent of the ideal residue for stage 3 computed using the slow but accurate ADC. The gradient descent approach (eqn. 1) is now used to estimate the parameter set (α, β) of the function block F = f(V) for stage 3. Once the parameters have been obtained, we can repeat the above process, in turn for stage 2 and stage 1, respectively. It can be shown that even if stages 5-8 are similar to the non-ideal stages earlier in the pipeline, the calibration algorithm works successfully, as confirmed by the simulation results. However, the accuracy of the parameter set depends on the resolution of the residue, which is quantised by the following stages in a pipeline. Therefore, we add a few extra stages at the end of the pipeline. The above algorithm for calibration is run in the background along with the normal conversion. Once the parameters have been estimated, we can implement the correction mechanism either in the analogue domain or in the digital domain.

![Graph showing INL error profile before and after calibration for op-amp gain of 800 and capacitor ratio mismatch of 3-10%](image)

Fig. 3 INL error profile before calibration and after calibration for op-amp gain of 800 and capacitor ratio mismatch of 3-10%.

a) Before calibration
b) After calibration

In the digital domain implementation of the correction mechanism, the correct estimate of the digital output can be computed recursively from the least significant calibrated stage until the MSB calibrated stage, by processing the non-ideal digital output of the pipeline with the set of parameters obtained by calibration. Thus, the whole algorithm for calibration and computation of the output is carried out in the digital domain with the use of few parameters, which requires few multiplications and additions, resulting in minimal hardware.

In an analogue domain implementation of the correction mechanism, we can implement the gain factor α by changing the reference voltages of the following stages in proportion to the gain parameter [5]. The offset parameter β can be implemented easily by modifying the conventional 1 bit switched capacitor circuit. One such modification involves the use of an extra capacitor to dump charge proportional to the offset parameter β during phase \( \phi_1 \).

Simulation results: An 8 bit resolution ADC has been simulated in MATLAB. There were 10 stages in the pipeline. Only the first four stages were calibrated. The op-amp gain was assumed to be constant over the input range and was ~300. The capacitor ratio mismatch in each stage was of the order of 5-10%. It is always assumed to be less than one to avoid missing decision levels. The complete simulation was stopped when all the stages needed calibration were calibrated for an 8 bit overall resolution. However, in a real-time scenario, the calibration cycle would be repeated to track the changes in the circuit parameters due to temperature and aging. A slowly varying ramp signal was used as the input signal for calibration. Fig. 3 shows the INL error profile before and after calibration. The error profile indicates that the INL is ±0.8 LSB and DNL is less than ±0.6 LSB as compared to the uncalibrated INL and DNL of 7 LSB.
Conclusions: A background technique for the calibration of pipelined ADCs has been proposed. This method has been shown to correct for all systematic non-idealities such as op-amp gain errors, capacitor mismatch and charge injection. The technique has been demonstrated to work for an 8 bit ADC using a MATLAB simulation.

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References

12nm tunable WDM source using an integrated laser array


A 12nm tunable source with up to 15mW fibre coupled power has been fabricated by integrating four DFB lasers and a booster amplifier to provide a single output. High-yield and low-cost techniques are used, such as quartz-wave-shifted phase-masks for wavelength definition and an integration technique with only two regrowths.

Introduction: Tunable laser sources are needed for wavelength division multiplexed (WDM) systems for a variety of applications. The market that can support the highest cost is the cold spare, where a single tunable source can temporarily be used to replace the source for a failed channel. This relatively low volume market can be addressed by fairly complex integrated or hybrid tunable sources [1]. A much higher volume market that can only support a marginal increase over current distributed feedback (DFB) laser costs is in WDM systems to obtain reconfigurability and eliminate inventory costs. As the number of channels increases, it becomes difficult to stock large numbers of unique lasers for each wavelength channel. The high price sensitivity of this market requires simple and robust approaches to obtain tunability. Since they are direct replacements for standard DFB lasers, tunable devices need to have the same output characteristics and be similar in cost. One of the most challenging parameters for tunable lasers has been output power, since conventional CW DFB lasers typically emit ~10mW into the fibre.

Although there have been a multitude of approaches to realising tunable sources, the long term wavelength stability of DFB lasers, their immunity to mode jumps and excellent spectral and noise characteristics has precluded the use of other architectures in practical systems [2]. An array of n DFB lasers, which increases the thermal tuning of each DFB laser by n, offers the same robust characteristics but with increased tunability [3].

Previous versions of single frequency lasers for use as tunable sources usually involved the use of directly-written gratings, possibly on-chip amplifiers, and a buried heterostructure geometry that typically needed four or more regrowths. These devices are relatively complex to manufacture, are physically quite large (~4mm), may have yield problems, or generally operate at low power levels [3 – 6]. The fibre coupled power, even with on-chip amplifiers, has generally been at or below 1mW. We report the fabrication and characterisation of DFB laser arrays which have a significantly reduced complexity, and process simplifications that permit greater yield and higher powers than previous DFB laser arrays and are suitable for use with external LiNbO3 modulators.

Design and fabrication: The layout of the chip is shown schematically in Fig. 1. The basic design uses ridge waveguides for both active and passive regions. Compared to buried-heterostructure devices, the DFB lasers have a wider stripe width and, together with the weak index confinement, the wavelength is much more tolerant of stripe width variations. Ridge lasers can also be very high power, helping to compensate for the 1/n combiner loss. A simple active/passive regrowth transition was employed to minimise the number of regrowths. In this process a passive buried waveguide runs continuously throughout the chip. The quantum wells and the grating layer are placed above this backbone. The grating layer is etched completely to form the amplifier, and both the grating and the quantum wells are removed in the passive section. The remaining difference between the active and passive sections is the second etch and regrowth of undoped InP in the passive p-cladding regions. An unguided region was included at the output of the chip to reduce reflections from the facet that can destabilise the DFB laser. In this region all the waveguiding layers are removed to allow the light to diffract only in the InP. Since there is no waveguide directly at the facet, light that is reflected does not efficiently couple back into the device.

As only one DFB laser is required to operate at one time, the four DFB lasers were placed only 50μm apart. The light from the 500μm long DFB lasers was combined using a multimode interference coupler with a length of ~230μm, and boosted with a 750μm long amplifier. The total chip length was 2.5mm and width 500μm.

Wavelength and singlemode yield can be a serious problem with DFB laser arrays. For singlemode operation from all lasers, as well as a simple manufacturable process, the devices used phase masks with a quarter-wave phase shift in the centre of the cavity. The phase mask process is similar to the three level process described in [7], but uses only a single intermediate masking layer of chromium. This was patterned with resist and formed a mask for reactive ion etching of the glass to a depth of ~0.25μm. The phase mask was illuminated at ~45° in a modified mask aligner forming an interference pattern between the first order and undiffracted beams. The ratio of the two powers in the fabricated phase masks was ~1:2.

Performance: Three sets of devices were fabricated: chips with no amplifier, chips with amplifiers and no unguided region, and chips with both amplifiers and unguided sections at the facets. Fig. 2 shows the light-current characteristics of a device with no integrated amplifier. The laser thresholds were 37–40mA, and about 1–2mW could be obtained in the fibre with a drive current of 150–200mA at temperatures between 10 and 40°C. There is about a factor of 8 difference between the fibre coupled power and the