speed of the algorithm significantly. Therefore, the card was not used for the main control algorithm, but was used to set the converter switching frequency, monitor-sensed voltages and currents, and establish an RS422 port. With the control law jumper in digital mode, the chopper operated, but was unable to maintain a nominal output voltage of less than 50%–100%–50% caused a transient in the output voltage (750 V from the nominal value. While paralleling the units... 

VI. EXPERIMENTAL RESULTS

The SSCM with analog control was found to satisfy all system specifications during each hardware test. A step load change of 50%–100%–50% caused a transient in the output voltage (750 V nominal) of less than ±7 V, as shown in Fig. 4. The transient performance of the two SSCM units operating in parallel is documented in Fig. 5 for a step load change of 100–150–100 kW. The output bus voltage transient decays rapidly with a variation of less than ±5 V from the nominal value. While paralleling the units at 200 kW, the output current was matched to within 1%. However, at 25 kW, which is near discontinuous conduction, the matching was only within 15%, but quickly improved to within 3.5% as the power level was increased to 50 kW. The mismatch at low power levels is more pronounced, since the converters were calibrated at full load. Consequently, there is a small variation in the droop slope between units.

Isolated units remained stable over all ranges of voltage and power. The units operating in the discontinuous region had significantly longer settling times and larger output voltage transients when given step load changes.

VII. CONCLUSION

The U.S. Navy has selected dc distribution and a more-electric approach for the 21st century surface combatant vessels. The SSCM is a crucial component in the DC ZEDS, and this first set of units has established a landmark for future endeavors. Control algorithms were evaluated based on specification requirements and implementation issues. DSP hardware was iteratively designed to meet all transient and paralleling requirements. Further, the units are now being retrofitted with a programmable universal controller that is TMS320 based. This will present a totally digital solution for the controller and allow flexibility in algorithm modification.

REFERENCES


RF Low-Noise Amplifiers in BiCMOS Technologies

Flora Carreto-Castro, Jose Silva-Martinez, and Roberto Murphy-Arteaga

Abstract—This paper deals with the design of low-noise amplifiers (LNA) fabricated in BiCMOS technologies. The LNA’s are based on an active inductor, which makes the topologies less sensitive to temperature variations and reduces the effects of process parameter tolerances. Experimental results show a 10-dB voltage gain at 1 GHz and unity-gain frequencies of 3.6 GHz. The noise figure, measured at 1 GHz, is 3.4 dB. The preamplifier has been fabricated using a 10-GHz BiCMOS technology.

I. INTRODUCTION

Due to the growing demand for monolithic radio frequency (RF) receivers for wireless communications, much attention has been paid to the design of low-noise amplifiers (LNA’s) and mixers.

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The paper is organized as follows. The active inductor is described in Section II. The LNA’s are introduced in Section III. In Section IV, small-signal transconduction, base–emitter resistance, base–emitter capacitance, and base–collector capacitance, respectively. For simplicity, we are neglecting the collector–emitter resistance and the parasitic capacitors associated with both collector and current source. At frequencies such that the effects of \( r_c \) and \( C_b \) can be neglected, and if \( R_i \gg 1/\omega C_b \), then \( R_i \) converts the input voltage to current and this current is integrated by \( C_e \). The voltage \( v_e \) is converted to current by the voltage controlled current source and fed back to the input. Since the collector current is larger than the base current, and considering the small-signal equivalent circuit shown in Fig. 2(b), the input impedance can be obtained as

\[
Z_i = \frac{v_i}{i} = \frac{1}{g_{m} R_i} \frac{1 + s R_i' C_e}{1 + s C_e C_b}.
\]  

Note that the input impedance of the next stage has not been considered in this analysis, it will be accounted for in the next section. For frequencies such that \( (R_i' C_e)^{-1} < \omega < (R_i' C_b)^{-1} \), (2) can be approximated as follows:

\[
Z_i \approx s R_i' C_e g_{m} \frac{s}{\omega_T} = sL_{eq} \quad (3)
\]

where \( \omega_T = 2\pi f_T = g_m / C_e \) is the transistor’s unity-gain frequency. In accordance with (3), at medium frequencies the structure behaves as an inductor. The inductance is proportional to \( R_i' \) and inversely proportional to the transistor’s unity gain frequency; these characteristics will be exploited in the next sections. For \( R_i' < 300 \Omega \) and \( f_T = 10 \text{ GHz} \), inductions in the range of 5–20 nH can be efficiently implemented. The low-frequency behavior of the inductor is limited by the zero located at \( (R_i' C_e)^{-1} \), for practical designs it is in the range 100–200 MHz. The high-frequency pole, at \( (R_i' C_b)^{-1} \), is typically around 2–3 GHz.


does the small-signal transconductances of OTA1 and OTA2, respectively. In this topology, the input voltage is converted to current by OTA1, and it is integrated by the capacitor; then the resulting voltage is converted to current by OTA2 and injected to the input. Based on this circuit, a grounded inductor can be implemented by the structure shown in Fig. 2(a). The behavior of the topology can be explained by exploring its simplified small-signal equivalent circuit depicted in Fig. 2(b).

In the equivalent circuit, \( R_i' \) represents the series of \( R_i \), and the transistor’s base resistance. The transistor’s parameters \( g_{m} \), \( r_e \), \( C_b \), and \( C_e \) are the small-signal transconductance, base–emitter resistance, base–emitter capacitance, and base–collector capacitance, respectively. For simplicity, we are neglecting the collector–emitter resistance and the parasitic capacitors associated with both collector and current source. At frequencies such that the effects of \( r_e \) and \( C_b \) can be neglected, and if \( R_i' \gg 1/\omega C_e \), then \( R_i' \) converts the input voltage to current and this current is integrated by \( C_e \). The voltage \( v_e \) is converted to current by the voltage controlled current source and fed back to the input. Since the collector current is larger than the base current, and considering the small-signal equivalent circuit shown in Fig. 2(b), the input impedance can be obtained as

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\[
Z_i \approx s R_i' C_e g_{m} \frac{s}{\omega_T} = sL_{eq} \quad (3)
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where \( \omega_T = 2\pi f_T = g_m / C_e \) is the transistor’s unity-gain frequency. In accordance with (3), at medium frequencies the structure behaves as an inductor. The inductance is proportional to \( R_i' \) and inversely proportional to the transistor’s unity gain frequency; these characteristics will be exploited in the next sections. For \( R_i' < 300 \Omega \) and \( f_T = 10 \text{ GHz} \), inductions in the range of 5–20 nH can be efficiently implemented. The low-frequency behavior of the inductor is limited by the zero located at \( (R_i' C_e)^{-1} \), for practical designs it is in the range 100–200 MHz. The high-frequency pole, at \( (R_i' C_b)^{-1} \), is typically around 2–3 GHz.
III. LOW-NOISE AMPLIFIERS

Based on the inductor of Fig. 2, a single-stage LNA can be implemented, as shown in Fig. 3. The inductor $L_c$ is used to match the input impedance, sometimes another inductor connected at the base of Q1 is also used [1]. By employing typical circuit-analysis techniques and considering that the active inductor is characterized by (3), the small-signal voltage gain can be shown to be

$$
\frac{v_o}{v_i} \equiv \frac{-\omega T_1 R'_{pe}}{\omega T_2 R'_L + s \left( 1 + \frac{1}{\omega T_2} \left( \frac{1}{C_{e2}} + \frac{R'_{pe}}{R'_L} \right) + s^2 \left( \frac{R'_p C_L}{\omega T_2} \right) \right)}
$$

(4)

where $g_{m1}$ is the transconductance of Q1, $R'_L$ is the equivalent input resistance (source resistance, base resistance of Q1, and emitter inductance reflected to the base); $R'_L$ and $C_L$ are the load resistance and load capacitance, respectively. Below the pole’s frequency, the voltage gain is determined by the ratio of resistors; hence it presents low sensitivity to temperature variations. Note from (4) that the voltage gain presents a low-pass behavior, wherein the frequency of the poles is given by

$$
\omega_p = \sqrt{\frac{\omega T_2}{R'_p C_L}} = \sqrt{\frac{1}{L_{oc} C_L}}.
$$

(5)

According to this expression, the higher the active inductance, the lower the amplifier’s bandwidth is. It is important to reduce the input capacitance of the next stage, otherwise the frequency response could be further degraded. From (4), the pole’s quality factor of the LNA is

$$
Q \equiv \frac{1}{1 + \frac{C_L}{C_{e2}} + \frac{R'_p}{R'_L}} \sqrt{\omega T_2 R'_p C_L}.
$$

(6)

Peaking effects in the voltage gain of the LNA are avoided if $Q < 1$, this can be easily guaranteed by increasing $R'_L$. If the first-stage’s voltage gain is not high enough, then a second stage can be used, as shown in Fig. 4.

For high gain amplifiers, the LNA’s noise level is dominated by the first stage [2]; in this case, the noise figure can be approximated as follows:

$$
NF \equiv 1 + \frac{r_{11}}{R'_S} + \frac{|Z_1 + r_{11} + R'_S|^2}{y_{m1}^2 |Z_1|^2} \left( \frac{2\eta I_{C1}}{4kT R'_S} \right)
$$

(7)

where

$$
Z_1 = \frac{1}{\omega C_{c1}}.
$$

In (7), we have considered that $I_{C1}$ is high enough ($>0.5$ mA). The noise figure is clearly limited by the base resistance $r_{11}$; in order to achieve low noise figures, small base resistance transistors and optimum input bias conditions are required. Because the active inductor is at the output of the LNA its noise contribution is reduced due to the gain factor, the LNA is biased using the technique proposed in [2], further details can also be found in [9].

IV. EXPERIMENTAL RESULTS

The low-noise amplifiers were fabricated in a 1.2-$\mu$m BiCMOS technology. A microphotograph of the chip is shown in Fig. 5. The single-stage and two-stage LNA’s are located at the right and left hand side of the microphotograph, respectively. For characterization purposes, several calibrating structures have also been included. Bias currents for transistors Q1 and Q2 were 2.5 and 1 mA, respectively. The inductance of $L_c$ is around 0.5 nH. The active area, including the pads, of the two-stage LNA is only 0.6 mm², the area of the entire chip is 2.2 mm². The preamplifiers are biased with a 3 V supply voltage.

Simulated results for the two-stage LNA, 15-dB voltage gain, have shown noise figures of 3.1 dB at 1 GHz, and input reflection coefficients of $-10$ and $-12$ dB at 1 and 2 GHz, respectively. Temperature simulations for $-50^\circ$, $27^\circ$, and $80^\circ$ have shown variations in the midband voltage gain of $\pm$1 dB. This result was expected because the maximum voltage gain depends on the ratio of resistors. For the same temperature variations, the 10-dB gain frequency varies within the range of 1.6–0.95 GHz; from (5), it can be noted that the frequency of the poles is more sensitive to temperature variations.

The measured voltage gain for the two-stage LNA, upon deembedding [10], is shown in Fig. 6. At medium frequencies, e.g., 0.5–1 GHz, the voltage gain is around 12.5 dB; the LNA was designed for 15-dB voltage gain. This error is due to the process parameters tolerances, especially in $R'_{pe}$. The voltage gain is larger than 10 dB for frequencies up to 1 GHz, while the unity gain frequency is 3.6 GHz. Experimental results for the bipolar transistors have shown unity gain frequencies of 9–10 GHz. The input reflection coefficient at 1 GHz is around $-8$ dB.

Fig. 7 shows the measured output spectrum for the two-stage LNA performed at the 1-dB compression level. According to this result, the input 1-dB compression level is around $-25$ dBm. The measured
noise figure at 1 GHz is around 3.4 dB, this value is in good agreement with the expected one. A summary of the results is given in Table I. Similar results have been obtained for the one-stage LNA but the voltage gain is limited to 8 dB [9].

V. CONCLUSION

An active inductor for high-frequency applications has been proposed. The inductor is based on the gyrator principle, and a resistor controls its inductance. Using this active inductor, two low-noise amplifiers have been designed. The performances of the two-stage’s LNA are comparable to previously reported structures but avoid the use of expensive technologies. For a voltage gain of 10 dB at 1 GHz, noise figures below to 3.4 dB have been achieved.

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REFERENCES