A BiCMOS Bluetooth/Wi-Fi Receiver


Analog & Mixed-Signal Center, Texas A&M University, College Station, TX, 77840, United States

Abstract — A fully integrated direct conversion receiver, supporting both Bluetooth and 802.11b standards, is implemented using IBM 0.25µm BiCMOS technology. The RF front-end is shared between both standards while the baseband blocks are programmable for each receiving mode. All the components of the receiver from the LNA to the ADC are integrated using 19mm² of silicon area. The current consumption of the chip is 41.3mA/45.6mA in Bluetooth/802.11b standard and the measured sensitivity is -91dBm/-86dBm, respectively.

Index Terms — Receivers, Wireless LAN, Bluetooth.

I. INTRODUCTION

Both Bluetooth and Wi-Fi standards operate at the same ISM band (2.4-2.483GHz). Wi-Fi is meant to be the wireless version of Ethernet, offering data rates up to 11Mb/s. On the other hand, Bluetooth is designed to replace cables that are used for relatively low speed data transfer, roughly up to 1Mb/s. Both standards complement each other in providing efficient wireless connectivity for most existing applications. A monolithic receiver, supporting both standards, is a cost-effective solution to enable broad wireless capabilities in a number of electronic products.

This paper presents a receiver, fully integrated from the LNA to the ADC, supporting the above-mentioned standards and fabricated using a 0.25µm BiCMOS process. The direct conversion architecture of the receiver, used in both standards, and a system level description are presented in section II. The RF front-end and the frequency synthesizer are described in detail in sections III and IV respectively. The operation of the programmable baseband blocks is discussed in section V. Experimental results are given in section VI and finally conclusions in section VII.

II. DUAL-MODE RECEIVER ARCHITECTURE

Most Bluetooth receiver implementations [1] use a low-IF architecture due to its small bandwidth and relaxed image rejection requirements. On the other hand, due to the large channel bandwidth in Wi-Fi, a direct-conversion receiver (DCR) is the best approach. Fundamentally, there are three possible architectures for a multi-standard Bluetooth/Wi-Fi receiver: (1) DCR for Bluetooth with Wi-Fi, (2) Low-IF for Bluetooth and DCR for Wi-Fi and (3) Low-IF for Bluetooth and Wi-Fi. The first combination is the best in terms of power consumption and, since both standards use the same architecture, the maximum level of building blocks sharing is attained. However, problems associated with using the DCR architecture for Bluetooth must be solved. In the second combination, each standard uses its most suitable architecture, which means easier implementation at the expense of increased cost because of the reduced sharing of building blocks. This approach has been used in [2, 3]. The third combination would demand high power consumption in Wi-Fi mode due to the large channel bandwidth.

In this design, direct conversion architecture (Figure 1) is used for both standards to achieve the lowest area and power consumption. Since both standards use the same RF frequency band, the RF front-end (LNA and mixer) is shared. The baseband blocks (LPF, VGA, and ADC) are reconfigurable according to the data rate, bandwidth and modulation format of each standard. In order to improve the receiver sensitivity, the gain of the RF front-end is set to 33dB, which is the maximum possible allowed by the adjacent channel level of -35dBm in the Wi-Fi standard. For a high input signal level, the LNA is bypassed and an attenuator is used to avoid saturation of the mixer input.

Due to the short preamble time in the Bluetooth standard, a single 24dB VGA step is used to minimize the receiver gain settling time. As a result, higher ADC resolution (11bits) is required in Bluetooth mode at a sampling rate of 1MHz. In 802.11b mode, the ADC runs at 44MSample/s. Using the same 11bits resolution would burn unacceptably high power. Therefore, the ADC resolution is lowered to 8 bits at the expense of finer VGA steps of 2dB.

![Figure 1. Dual Mode Receiver Block Diagram](image-url)
III. FRONT-END

The BiCMOS LNA shown in Figure 2 is an inductive degenerated differential structure that provides a gain of 15dB. A differential attenuator is implemented in parallel with the LNA as indicated in the dashed box in Figure 2; it is a resistor divider built with NMOS transistors and provides an attenuation of 15dB. In high gain mode, the transistors of the attenuator (M5-M9) are turned off by connecting their gates to ground, thus, the normal operation of the LNA is not affected. For low gain operation M5-M9 are driven into triode region, the bias current of the LNA (I_tail) is turned off and the impedance matching is assured through capacitor Cm.

NMOS transistors were chosen for the RF drive stage of the LNA (M1, M2) due to the fact that they achieve better linearity than their bipolar counterparts for a given bias current. Bipolar transistors are preferred as cascode devices (Q1, Q2) because of their larger transconductance, which minimizes the voltage gain from gate to drain of M1 and M2 and, in turn, reduces the Miller effect and improves reverse isolation. Degenerative inductor Ls (1nH) and load inductor Ld (3nH) are on-chip planar spiral inductors. They are formed using the topmost metal and there is deep trench lattice pattern beneath them to reduce metal loss and substrate loss respectively. All the matching conditions are established on-chip using inductive source degeneration technique [4]. The only required off-chip component is a 1:1 balun to perform the single-ended to differential conversion for the RF signal.

The mixer shown in Figure 3 is a fully differential Gilbert-cell based structure with I and Q branches sharing the same RF drive stage, therefore eliminating the mismatch present in the conventional down-conversion structure employing two separate I/Q mixers. The current commutating switches are NPN bipolar transistors which require less LO drive power than NMOS transistor switch pairs. The RF driving stage uses NMOS transistors for better linearity.

Figure 3. Mixer Schematic

IV. FREQUENCY SYNTHESIZER

An integer-N frequency synthesizer is used to generate the local oscillator (LO) signal, as shown in Figure 4. Since Bluetooth and Wi-Fi use the same frequency band, the only restriction imposed on the design for dual-mode operation is to generate the frequencies corresponding to the channels of both standards. The phase noise and settling time specifications for Bluetooth are considered for the design since they are more stringent than the ones for Wi-Fi.

The VCO is operated at twice the desired output frequency. This implies a 10%-15% larger power consumption in the VCO and prescaler compared to the VCO running at 2.4GHz. This extra power consumption is justified since quadrature generation can be performed through a divide-by-two flip flop, which is known to have very good quadrature accuracy [5]; in this way, the VCO does not need to drive passive phase shifters, which introduce a large attenuation to its output.

The charge pump, is implemented using cascode current mirrors to reduce the dependence of the output current on the output voltage. The resulting current mismatch is smaller than 0.5%. The drawback of using cascode current mirrors is a reduced compliance voltage at the output of the charge pump, however, this problem is not critical due to the relatively high gain of the VCO (300 MHz/\text{V}).

Figure 4. Frequency Synthesizer Block Diagram
In order to achieve high spurious suppression, the loop bandwidth is reduced as much as the settling time requirement allows. By doing so, the loop filter yields a very large capacitor C1 (340pF). A completely integrated solution is desired but the large area required by the capacitor is prohibitive. To allow integration of the capacitor, a capacitance multiplier is used in the loop filter [6]. Figure 5 shows the schematic diagram of the capacitance multiplier, which is based on an impedance scaler. Through this technique, for a given voltage variation in node A, a current variation M times larger than the one provided by C alone is obtained. This larger current variation represents an equivalent smaller impedance seen from node A. For a capacitive impedance, this means a larger equivalent capacitance.

![Capacitance Multiplier Schematic Diagram](image)

The VCO is implemented with an LC-tuned negative gm oscillator. The base nodes of bipolar transistor drivers are AC-coupled with oscillating nodes and biased by an extra DC biasing circuit to keep the transistors out of the triode region. Although the biasing circuit contributes to base resistance, improved linearity helps to reduce the overall phase noise. Special low resistance top metal layer is utilized for the on-chip inductor. Simulated quality factor of the 1.5nH inductor is 13. The intrinsic base-collector diode present in bipolar devices is used as a varactor, which provides ±17% capacitance variation range.

![VCO Circuit Schematic](image)

The prescaler employs an enhanced switching topology [7] that eliminates the possible glitches generated during phase switching. The VCO output frequency is divided by eight using three cascaded asynchronous D flip-flops (DFF) connected in a master–slave configuration.

The third stage of the cascaded dividers of the prescaler is formed by two DFFs driven by the quadrature outputs of the second divider. This configuration provides 8 different phases, separated by 45° each, at the output of the third stage. These phases are fed into an 8:1 multiplexer that selects a phase that is applied to the last asynchronous divide-by-two that forms the 15/16 prescaler. The prescaler is followed by a programmable swallow counter that sets the desired channel at the output of the VCO.

### V. BASEBAND SECTION

The dual-mode channel selection filter is implemented as an OTA-C 5th order, Butterworth low pass structure. It is formed by two cascaded biquadratic sections preceded by a low pass pole implemented with passive RC elements; the out-of-band signals are attenuated before the active stages of the filter, thus improving the IIP3. The same filter is used for both standards by programming the cut-off frequency; 600 kHz for Bluetooth mode and 6MHz for Wi-Fi mode.

The employed OTA is an emitter-degenerated bipolar differential pair with current scaling. Dual-mode operation is achieved by switching the emitter-degeneration resistors, fine frequency-tuning is achieved by using a bank of capacitors to account for process and temperature variations. The bias current is inversely scaled with the same factor as the emitter-degenerated resistance R, to keep the voltage drop across R constant, in both modes. This results in the same linearity performance and optimized power consumption for both modes.

The VGA is implemented using the OpAmp-R technique, where the resistors are switched to control the gain. In Wi-Fi mode, the VGA operates with 3 stages to provide a gain range of 62dB in steps of 2dB. In Bluetooth mode, only the last stage is activated to provide a single gain step of 24dB. RC high pass filters (HPF) are used to reject DC offsets and prevent the VGA stages from saturation. Each VGA stage is designed such that its output referred offset is constant regardless of its gain to avoid the slow response of the HPFs [8].

A time-interleaved pipeline ADC with programmable resolution (8bits/11bits) and sampling rate (11MHz/44MHz) is implemented to support both Bluetooth/802.11b receiving modes. The sampling frequency is adjusted by the number of active interleaved ADC branches and the dynamic range is controlled by the number of active pipeline stages.

521
VI. EXPERIMENTAL RESULTS

The receiver IC has been fabricated using IBM 0.25μm BiCMOS technology. The die microphotograph is shown in Figure 7. The receiver area including pads is 19mm², from which about 50% is occupied by the ADC. The phase noise from the local oscillator and the BER performance of the receiver are shown in Figures 8 and 9, respectively. A summary of the experimental results is presented in Table 1.

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>BT</th>
<th>WiFi</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity</td>
<td>-91dBm</td>
<td>-86dBm</td>
</tr>
<tr>
<td>IIP3</td>
<td>-13dBm</td>
<td></td>
</tr>
<tr>
<td>IIP2</td>
<td>-10dBm</td>
<td></td>
</tr>
<tr>
<td>Input S11</td>
<td>&lt;11dB</td>
<td></td>
</tr>
<tr>
<td>LO Phase Noise</td>
<td>-120dBc/Hz at a 3MHz offset</td>
<td></td>
</tr>
<tr>
<td>Rx active current</td>
<td>41.3mA</td>
<td>45.6mA</td>
</tr>
<tr>
<td>Rx active current (without ADC)</td>
<td>27.9mA</td>
<td>30mA</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>2.5V</td>
<td></td>
</tr>
</tbody>
</table>

Table 1. Summary of Experimental Results

VII. CONCLUSION

A dual-mode receiver supporting both, Bluetooth and 802.11b standards, has been designed, implemented and tested. The unique features of this design include full integration of the receiver from LNA to ADC, the use of a single direct conversion architecture for both standards and programmability of all the baseband blocks. With respect to previously reported dual mode solutions [2, 3], this design achieves better sensitivity in Bluetooth mode and lower power consumption for both modes.

ACKNOWLEDGEMENTS

Authors thank the MOSIS service for its support in the fabrication of the IC and the RF IC design group from Texas Instruments for technical discussions.

REFERENCES